2011

Built-In Self-Test Solution for CMOS MEMS Sensors

Iftekhar Basith
University of Windsor

Built-in Self-Test Solution for CMOS MEMS Sensors

by

Iftekhar Ibne Basith

A Thesis
Submitted to the Faculty of Graduate Studies
through the Department of Electrical and Computer Engineering
in Partial Fulfillment of the Requirements for
the Degree of Master of Applied Science at the
University of Windsor

Windsor, Ontario, Canada

2011

Built-in Self-Test Solution for CMOS MEMS Sensors

by

Iftekhar Ibne Basith

APPROVED BY:

_____

Dr. Nader Zamani, External Reader
Department of Mechanical, Automotive, and Materials Engineering

_____

Dr. Mitra Mirhassani, Departmental Reader
Department of Electrical and Computer Engineering

_____

Dr. Rashid Rashidzadeh, Co-Advisor
Department of Electrical and Computer Engineering

_____

Dr. Majid Ahmadi, Co-Advisor
Department of Electrical and Computer Engineering

_____

Dr. H. Wu, Chair of Defense
Department of Electrical and Computer Engineering

August 18, 2011

DECLARATION OF ORIGINALITY

I certify that, to the best of my knowledge, my thesis does not infringe upon anyone's copyright nor violate any proprietary rights and that any ideas, techniques, quotations, or any other material from the work of other people included in my thesis, published or otherwise, are fully acknowledged in accordance with the standard referencing practices. Furthermore, to the extent that I have included copyrighted material that surpasses the bounds of fair dealing within the meaning of the Canada Copyright Act, I certify that I have obtained a written permission from the copyright owner(s) to include such material(s) in my thesis and have included copies of such copyright clearances to my appendix.

I declare that this is a true copy of my thesis, including any final revisions, as approved by my thesis committee and the Graduate Studies office, and that this thesis has not been submitted for a higher degree to any other University or Institution.

ABSTRACT

A new readout circuit with integrated Built-in Self-Test (BIST) method for capacitive Micro-Electrical-Mechanical System (MEMS) devices using charge-control method has been proposed, developed and fabricated in which the input stimuli for the Device Under Test (DUT) is current source. A precision Time-to-Digital Converter (TDC) is used to measure the converted time domain signals from the output of the DUT. The proposed scheme is self-calibrated to reduce the need for external equipments and performs well under process, supply and temperature variations. A comb drive was designed for the simulation purpose and results indicate that the proposed method can successfully measure and detect minor structural defects altering the MEMS nominal capacitance. Post layout simulation was performed with the extracted view in Cadence environment and the results were in accordance with the expectation. The proposed design has been developed using tsmc65nm technology. The fabricated chip has been tested and measurement results are also included in the thesis.

DEDICATION

Dedicated to my respected parents whose prayers are always with me to guide, my loving wife Israt Jahan who inspires and encourages me in every steps of my life and my loving daughters Faiza and Fareeha whose smiles and hugs always boosts me whenever I face any stressful and pressure situation.

ACKNOWLEDGEMENTS

First I want to thank the Almighty Allah for passing me through the research work easily and allowing me to fulfil the requirements without difficulty.

Secondly, I want to thank my honourable and knowledgeable advisors, Dr. Rashid Rashidzadeh and Dr. Majid Ahmadi for their constant support, constructive feedback and strict guidance. Without their experience in IC design, and knowledge on SoC (System on Chip) this project would not have been a success with the tight deadline provided by the CMC for fabrication of the chip. I am deeply grateful to Dr. Rashid for the amount of time he dedicated for me and this project including weekends and even the evenings and nights of regular work week.

Thirdly, I want to thank my honourable committee members for their thoughtful modifications and inputs regarding the thesis work during my first and second seminars.

I want to thank the CMC fabrication team for their steady and ongoing service during the fabrication phase. Their prompt response to some of the problems I faced while designing the chip, allowed me to proceed without any major problem.

I want to thank my colleagues and co-workers in the RCIM lab, especially Nabeeh Kandalaft and Tareq Muhammad Supon for their valuable criticism, helpful attitude, and strong support towards my work.

I want to mention the amount of support I received from the departmental stuffs Andria Ballo and Shelby Marchand regarding the administrative and bureaucratic ideas.

Finally I want to thank my parents, my wife and my daughters for their everlasting and wonderful love by supporting me in each stage of my work and cheering me up to go for the higher studies.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER I

INTRODUCTION

By developing a micromachined electrostatic motor in 1987 [1], Berkley Sensor and Actuator Center, University of California triggered a new era of Micro Electro Mechanical System (MEMS) design. Since then, the CMOS-MEMS integration [2] has emerged as a better mean for performance improvement of Microsystems significantly while reducing the fabrication cost. Hence, electro-mechanical systems with analog and digital modules are now being integrated on a single chip to produce high performance.

1.1 Capacitive MEMS

Capacitive MEMS structures have relatively simple architectures with some added advantage over the traditional counterparts.

- MEMS devices provides high function density within a tiny space, weight generally falls into nano-gram range.
- Due to very small sensing structure MEMS devices can achieve high resolution.
- Energy consumption is usually one tenth of the conventional devices while the speed is ten times more.
- Signal delay can be minimized for better compatibility of its mechanical and electrical interface.
- The fabrications cost is much lower than the conventional devices, as they can be fabricated in batches and on the same chip with VLSI circuits.

Capacitive MEMS sensors mainly operate based on the principle of capacitance variation where parameters of interest such as acceleration, ultrasonic waves and pressure

are first converted to electrical signals by a MEMS structure and then the generated signals are measured by a readout circuit.

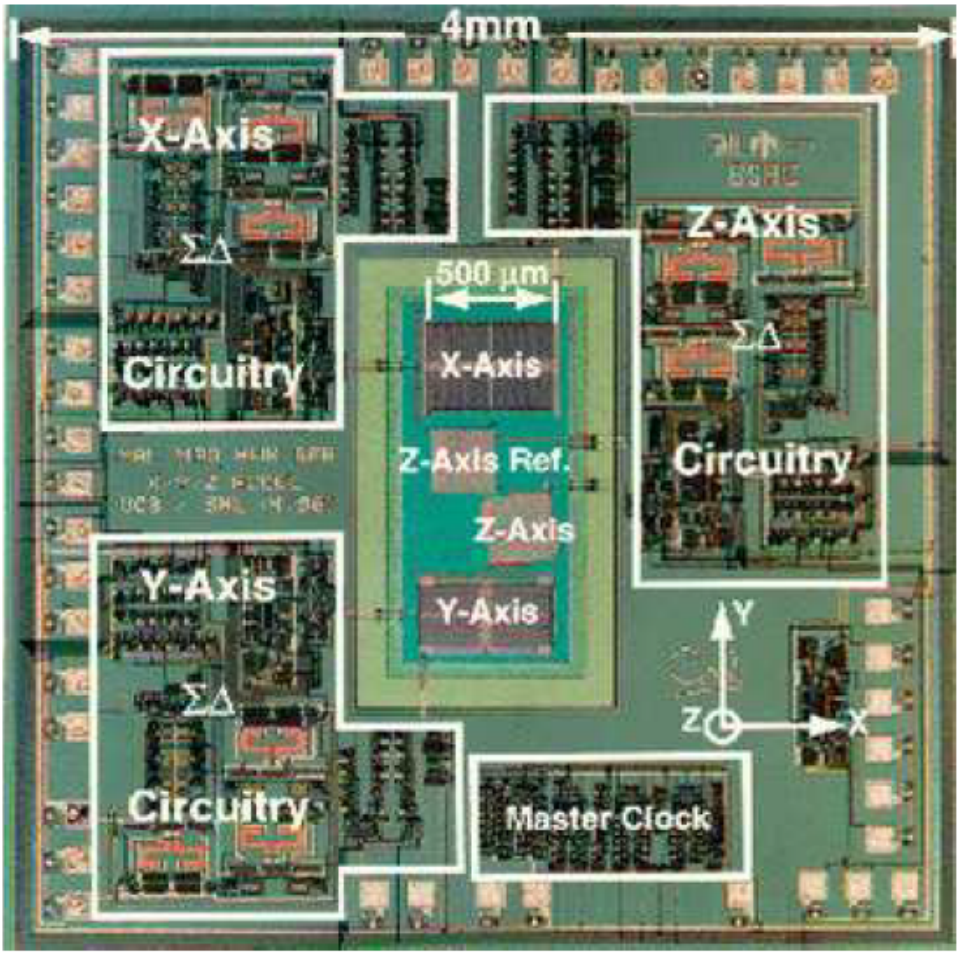


Fig 1.1 Photo of ADXL250 accelerometer by Analog Devices Inc. [3]

1.2 Built-In Self-Test for MEMS sensors

Built-in self-test (BIST) is the technique of designing additional hardware features into integrated circuits to allow them to perform self-testing. There are two main techniques to conduct test on MEMS sensors: (a) voltage control and (b) charge control. Various researchers have used voltage control techniques. A symmetrical test method is

proposed in [4], where the central mass (movable capacitance plate) of the MEMS structure is partitioned into two symmetrical portions. The responses of these symmetric parts to identical stimulus inputs are captured and compared to each other. If the difference between the responses exceeds a certain tolerance level a physical defect is reported. This method does not require test stimulus calibration and it can detect most of the structural defects. However, a perfect structural symmetry requirement limits the application of this method. This method also cannot be applied to detect some global defects affecting both sides of the symmetrical structure concurrently.

Sensitivity test method can also be used to perform test on MEMS structures [5] - [7]. In this method, the Device Under Test (DUT) is activated to its full working range through appropriate external test input stimuli and then the response of the DUT is captured and compared against the signature of a fault free device. This test method can be applied to any MEMS structure to detect possible parametric and catastrophic faults. It is evident that precise input stimuli generator and response evaluator are required to successfully detect DUT faults in this method, thus limiting its application for in-field tests. In [7], the symmetry and sensitivity BIST methods are integrated in one circuit where the fixed capacitance plate is partitioned into symmetric structure.

1.3 Proposed Work

In this thesis a new readout and built-in self-test solution for MEMS sensors is proposed and developed which has the capability of self-calibration. In the proposed scheme, instead of commonly used voltage controlled stimuli, charge controlled stimuli have been employed to cover a wide range of MEMS structural defects. The proposed BIST method has several advantages over the current voltage-control based solutions: (a)

hard-to-detect faults can be covered without risking the structural collapse due to excessive electrostatic force; (b) external costly equipments are not needed for calibration due to an employed self-calibration technique.

In the proposed test method, the Device Under Test (DUT) is charged and discharged by current sources. This mechanism varies the electrostatic force between the DUT plates changing the associated capacitance of the DUT. The variation in the capacitance is captured and converted to time intervals and then digitized by a Time-to-Digital Converter (TDC).

The rest of the thesis is organized as follows: background study and review of literature is presented in chapter II. The block diagram of the proposed BIST circuitry along with the functions of the building block is discussed in chapter III. Chapter III also elaborates the principle of the proposed measurement method with mathematical justification and the adopted self-calibration technique. Chapter IV describes the fabrication of the DUT and test circuitry along with the schematic, post layout simulation results and experimental measurement results. Chapter V finally concludes the thesis with some discussion and future works.

CHAPTER II

REVIEW OF LITERATURE

With the three-dimensional integrated circuits on the horizon, the prospect of successful CMOS and MEMS integration has come closer to the reality. CMOS-MEMS integration [2] improves the performance of Microsystems significantly while reducing the fabrication cost. However, due to the multi dimensional nature [9] of such systems, robust and advanced test methodologies are needed to address the potential challenges ahead. MEMS sensors operate mainly based on the principal of capacitance variations where the parameters of interest such as acceleration, ultrasonic waves and pressure are converted to electrical signals by a variable capacitor formed by MEMS structure. The signals generated by MEMS structure are then measured by a readout circuit. Hence, the accuracy and resolution of readout circuits also play an important role on the overall performance of MEMS sensors.

2.1 Built-In Self-Test

BIST circuits allow the DUT to evaluate its own quality without elaborate automated test equipment (ATE). A BIST circuit may require little more than a power supply and a master clock from the tester. Since the DUT testes itself using BIST, a much less expensive ATE tester can be used. BIST have several advantages to offer:

1) It lowers the cost for testing by avoiding the need for advanced external ATE.

2) Since special test structures can be incorporated into the chips, BIST provides better fault coverage.

3) Test times can be shortened by designing and implementing BIST techniques.

4) The consumers themselves can test chips during in-field usage.

MEMS devices are now fabricated on the same chip (SoC) with digital, analog, memory, and FPGA circuit technologies. Hence, a thorough and effective testing solution for MEMS devices is needed to ensure fault free functioning. However, due to the great diversity of MEMS structures and their working principles, various defect sources and multiple field coupling MEMS testing is very challenging [9]. Built-in self-test is believed to be the promising solution for MEMS testing. A variety of BIST methods have been proposed in the literature for capacitive MEMS devices.

A symmetrical test method for MEMS sensors is proposed in [4] where the MEMS structure is partitioned into two symmetrical portions. The responses of these symmetrical parts to identical stimulus inputs are captured and compared with each other. When the difference between the responses exceeds a certain tolerance level a physical defect is reported. This method does not require test stimulus calibration and can detect most of the structural defects. However, this approach requires a perfect symmetrical structure limiting its application and it fails to detect faults when identical global defects exist at both sides of the symmetrical segments.

In [5] - [7] a test solution called sensitivity test is proposed. In this method, the MEMS structure is activated to its full working range through appropriate external test input signal. The response of the Device Under Test (DUT) is captured and compared against the signature of a fault free device. This test method, which is similar to the functional test of analog circuits, can be applied to any MEMS structure to detect possible parametric and catastrophic faults. It is evident that a precise input stimuli

generator and response evaluator are required to successfully detect the DUT faults in this method. Both the symmetry and sensitivity BIST methods are integrated by partitioning the fixed capacitance into symmetric structure in [7]. However, the stimulus input still is voltage and risk the structural collapse of the DUT.

2.1.1 Basic Capacitive MEMS Devices and Sensitivity BIST Method

A typical MEMS differential capacitance structure is shown in Figure 2.1. Movable plate is denoted by M, fixed plates are denoted by F1 and F2, while B1 and B2 are both beams of the MEMS device. As shown in Figure 2.1, the movable plate M constitutes differential capacitances C1 and C2 with the top and bottom fixed plates respectively. At rest, movable capacitance is at the centre and both C1 and C2 have the same value:

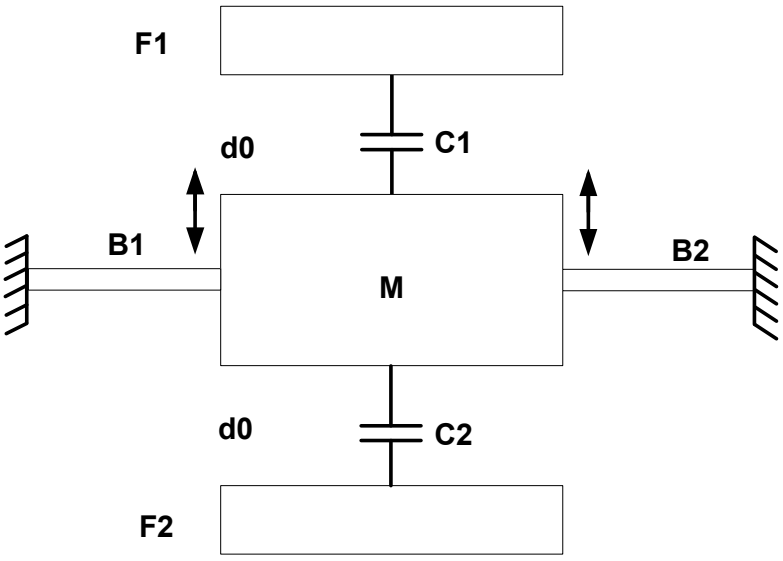


Figure 2.1: Basic schematic of a capacitive MEMS structure [7]

$$C1 = C2 = \frac{\varepsilon_0 A}{d_0} \tag{2.1.1}$$

Where, ε_0 is the dielectric constant of air, A is the overlap area between movable and fixed plates, and d_0 represents the static capacitance gap between them. A vertical stimulus will activate the MEMS structure and a certain displacement of movable plate M will occur along the vertical direction. Assuming the central movable mass moves upward with a displacement of x, the associated capacitances C1 and C2 under the test stimuli can be derived by

$$\mathrm{C1} = \frac{\varepsilon_0 A}{(d_0 - x)} \tag{2.1.2}$$

$$\mathrm{C2} = \frac{\varepsilon_0 A}{(d_0 + x)} \tag{2.1.3}$$

If V_0 represents voltage amplitude, ω denotes the frequency and t denotes the time then the positive modulation voltage $V_{mp} = V_0 sqr(\omega t)$ and negative modulation voltage $V_{mn} = -V_0 sqr(\omega t)$. They are applied to the fixed plates F1 and F2 respectively. But according to the charge conservation law, charges in C1 must be equal to C2.

$$\mathrm{C1}(\mathrm{V_{mp}} - V_M) = \mathrm{C2}(\mathrm{V_M} - V_{mn}) \tag{2.1.4}$$

Solving the above equations for sensing voltage at movable plate, V_M we have the following relation:

$$V_M = (x/d_0) V_0 sqr(wt) \tag{2.1.5}$$

From equation (2.1.5), it is evident that the central movable plate M acts just as a voltage divider between F1 and F2. By measuring V_M, we can find the displacement x of the central movable plate M, which is directly proportional to the physical stimuli. Thus,

we can derive the value of the applied physical stimuli. In the sensitivity BIST mode, driving voltage V_d is applied to the driving plate to mimic the action of the physical stimulus with electrostatic force. Then the central movable mass will experience an electrostatic attractive force F_e which is expressed as:

$$\mathrm{F_e} = \frac{\varepsilon_0 A V_d^2}{2d^2} \tag{2.1.6}$$

The response of the device to this electrostatic force is captured in the BIST mode, measured and compared with the good device response to check whether the device is faulty. This is the basic idea for the sensitivity test mode of a capacitive MEMS device. However, for vertical electrostatic driving, the driving voltage cannot exceed a threshold value called the collapse voltage by which the deflection exceeds 1/3 of the initial capacitance gap d_0. Otherwise, the movable plate will collapse causing a permanent damage to the structure. This is in fact the disadvantage of using voltage inputs as test stimuli for MEMS sensors.

2.1.2 Symmetry BIST Method

For symmetry test scheme, the fixed capacitance plates are divided into symmetrical portions. S1-S4 is fixed plates as shown in Figure 2.2. The basic idea behind symmetry test scheme is to check whether the two symmetric capacitances that is, C1and C2 in Figure 2.2 on the same side of the movable microstructure remain equal all the time, after the MEMS structure is excited by input voltage stimulus. Fixed plates S1 and S2 lie at the same side of the movable plate M. The capacitance between M and S1 is defined as C1 and between M and S2 is defined as C2. Two inputs of positively

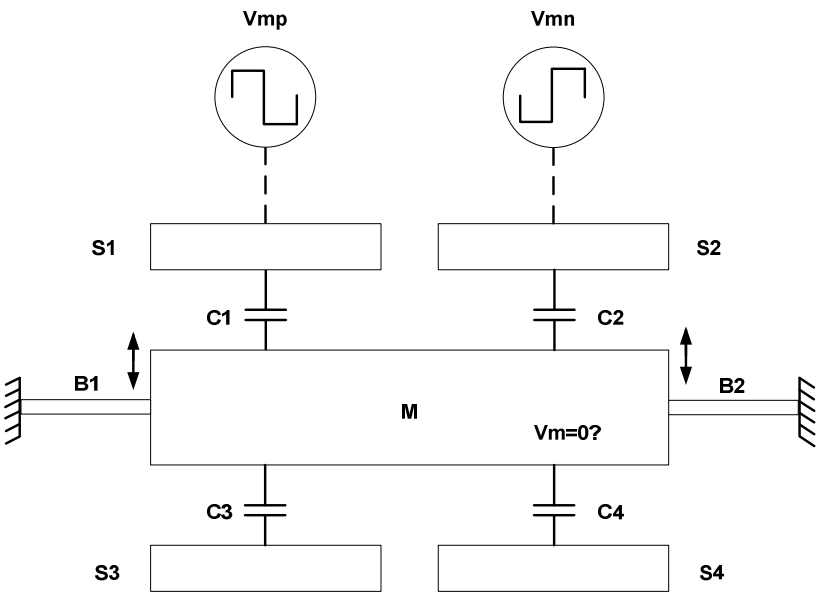


Figure 2.2: MEMS structure for Symmetry test scheme [7]

modulated V_{mp} and negatively modulated V_{mn} are applied to S1 and S2 separately. For fault-free devices, regardless whether the movable plate is in steady state or excited, C1 and C2 remain equal. If the voltage level on M is V_M, the charge conservation law states that charge Q1 on C1 and Q2 on C2 must also be equal.

$$C1\left(V_{mp} - V_M\right) = C2\left(V_M - V_{mn}\right) \tag{2.1.7}$$

Replacing $V_{mp} = -V_{mn}$ in equation (2.1.7), the final expression for sensing voltage is:

$$V_M = V_{mp}\frac{\left(C1 - C2\right)}{\left(C1 + C2\right)} \tag{2.1.8}$$

From equation 2.1.8 it is evident that when C1 equals C2, we have $V_M = 0$. This means if the symmetry is preserved, sensing voltage on the central movable plate is always zero for good devices. However, if the symmetry of the device is altered due to any local defect, the movable plate will tilt and C1 will not be equal to C2 and thus the

output voltage V_M will not be zero anymore. So, the value of output voltage on movable plate can easily be used as an indication of the device test result. In addition the polarity of V_M can also define which side of the two symmetric structures has the fault. For example, a stiction defect in the right side of the mass would cause C2 to be smaller than C1 and V_M will have the same phase polarity as V_{mp}, and vice versa. Similar verification can be done for both bottom capacitances C3 and C4 in figure 2.2.

2.1.3 Dual-Mode BIST Method

In the Dual-Mode BIST technique [6] for capacitive MEMS devices, the fixed capacitance plate(s) at each side of the movable microstructure are divided into three portions: one for electrostatic activation and the other two equal portions for capacitance sensing. As shown in Figure 2.3, M is the movable plate, D1 and D2 are the fixed driving plates, while {S1, S2, S3, S4} are the fixed sensing plates.

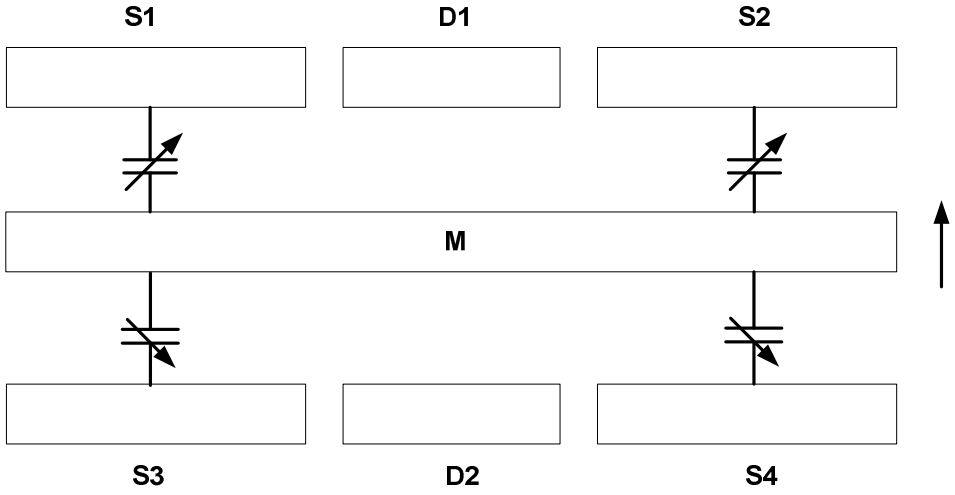
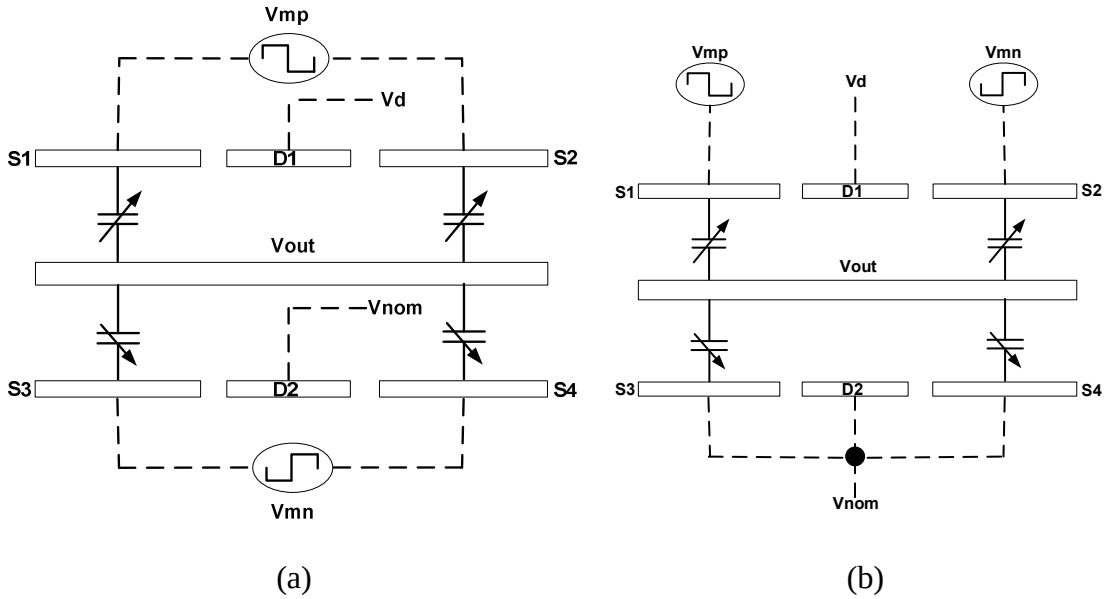


Figure 2.3: Fixed-plate partition for dual-mode BIST operation [7]

In sensitivity BIST mode, the test drive voltage V_d is applied to activate the DUT. Both the positive V_{mp} and negative V_{mn} modulation voltages are applied to the partitioned fixed plates {S1, S2} and {S3, S4} respectively (Fig. 2.4 a). The output voltage V_{out} of the DUT is measured for sensitivity analysis, and then compared with pre-calculated value within a tolerance level to determine whether the device is fault free or defective.

For the symmetry BIST mode, V_{mp} is applied to S1 and V_{mn} is applied to S2 (Fig. 2.4 b). In the same manner, V_{out} of the movable plate is measured. A nonzero response indicates a local defect causing the asymmetry of the DUT. An approximation can also be made about the location of the defect based on the value and polarity of the output.



(a) (b)

Figure 2.4: Voltage biasing for dual-mode BIST scheme (a) Sensitivity (b) Symmetry [7]

2.2 Readout Circuit

Readout circuits have been studied extensively for a long time. The principle of capacitance-to-voltage (C-V) conversion is the dominant method to design readout

integrated circuits (ROIC) based on the conventional Analog-to-Digital Conversion (ADC). These circuit structures have the advantage of high Signal-to-Noise Ratio (SNR), and high sensitivity [9] - [11]. As the supply voltage scales down, the conventional ADC method presents some drawbacks such as high power consumption and circuit complexity [10] - [12]. To increase the resolution, new approaches have been presented based on the conventional Time-to-Digital Conversion (TDC).

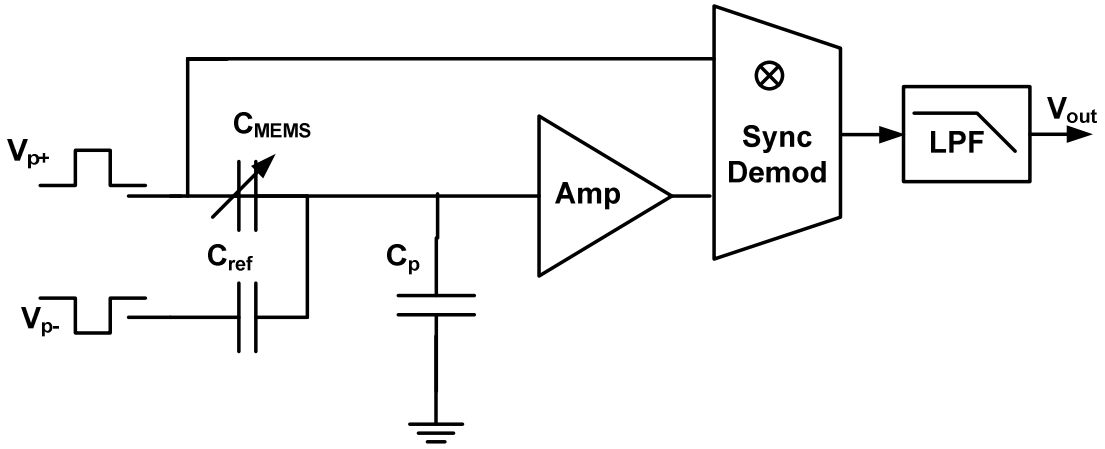


Figure 2.5: AC-bridge configuration for read out circuits [12]

2.2.1 AC-bridge with voltage amplifier

AC-bridge with voltage amplifier configurations [13] - [16] have a half-bridge formed with a MEMS (C_{MEMS}) and a reference (C_{ref}) capacitor, as shown in Fig. 2.5, and is driven by two AC signals with 180 degree phase difference. The output voltage is [12]:

$$\mathrm{V_{out}} = V_p \frac{\Delta C}{2C_{MEMS,0} + C_p} \times A_v \tag{2.2.1}$$

Where, A_v is the amplifier gain, V_p is the drive voltage amplitude, C_p is the parasitic capacitance, $\Delta C = C_{MEMS} - C_{ref}$ and $C_{MEMS,0}$ is the MEMS capacitor at rest.

However, the minimum detectable capacitance is determined by the thermal noise floor of the circuit and is still a function of parasitic capacitance [12]:

$$\Delta C_{\min} = \frac{2C_{MEMS,0} + C_p}{V_p} \times V_{n,rms} \times \sqrt{BW} \tag{2.2.2}$$

Where, $V_{n,rms}$ is the input-referred thermal noise of the amplifier and BW is the capacitance detection bandwidth.

2.2.2 Transimpedance amplifier

The second group of readout schemes [17] has similar configuration as ac-bridge ones (see Fig. 2.6), except for the fact that, one resistive feedback (R_f) is introduced, and the drive signals need to be sinusoidal to avoid distortion. The output voltage is:

$$\mathrm{V_{out}} = 2\pi f_{drive} V_m R_f \Delta C \tag{2.2.3}$$

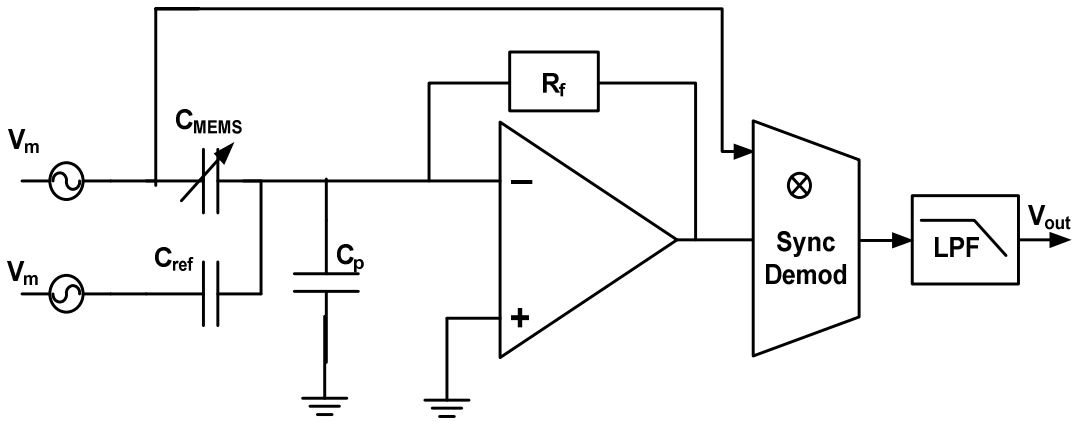


Figure 2.6: Transimpedance amplifier [12]

Where, f_{drive} is the drive voltage frequency, $\Delta C = C_{MEMS} - C_{ref}$ and V_m is the drive signal amplitude. However, the poles associated with R_f limits the bandwidth and the amplifier dominant pole creates an inductive effect. The thermal noise of the feedback resistor dominates the noise performance instead of the amplifier and the minimum detectable capacitance is derived as follows [12]:

$$\Delta C_{\min} = \sqrt{\frac{2k_B T\left(2C_{MEMS,0} + C_p\right)}{\pi GBW_{amp}}} \times \frac{\sqrt{BW}}{V_m} \tag{2.2.4}$$

Where, GBW_{amp} is the amplifier gain bandwidth and $k_B = 1.38066 \times 10^{-23}\, J/K$ is the Boltzmann constant.

2.2.3 Switched capacitor circuit

In the third group [12], [18] - [22] of readout circuits, an input capacitive feedback (C_{int}) is introduced (see Fig 2.7), which contains a packet of charge proportional to ΔC. The minimum detectable capacitance is expressed as below [12]:

$$\Delta C_{\min} = \sqrt{\frac{1}{f_s}} \times \left[\sqrt{\frac{16K_B T\left(2C_{MEMS,0} + C_p\right)C_{\text{int}}}{C_{out}}} \right] \times \left(\sqrt{BW}\right) \tag{2.2.5}$$

Where, C_{out} is the total amplifier output capacitance and f_s is the sampling frequency.

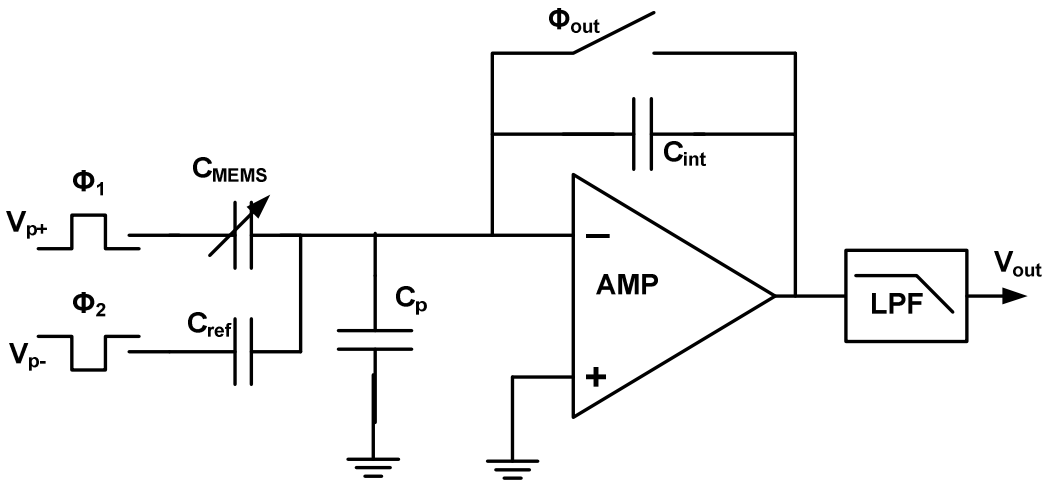


Figure 2.7: Switched capacitor configuration for readout circuits [12]

2.2.4 Comparison of the readout circuits

The performance of the above mentioned capacitive readout circuits were compared using the mentioned equations. It can be said, when the parasitic capacitance is very low then the ac-bridge circuit is able to detect very low capacitance change, whereas if the parasitic capacitance is high, the switched capacitor and trans-impedance amplifier circuits have better performance. Readout circuits in general should provide fine measurement resolution. However, PVT (Process, Voltage and Temperature) variations can affect the performance considerably.

CHAPTER III

BIST SOLUTION BASED ON CHARGE CONTROL TECHNIQUE

In this section, the block diagram and working principle of the proposed method will be investigated. In the proposed test method, the Device Under Test (DUT) is charged and discharged by current sources. This mechanism varies the electrostatic force between the DUT plates changing the associated capacitance of the DUT. The variation in the capacitance is captured and converted to time intervals and then digitized by a Time-to-Digital Converter (TDC) for evaluation. The chip has been fabricated using TSMC CMOS 65nm technology.

3.1 Proposed Block Diagram of Charge Control Method

The simplified block diagram of the proposed BIST architecture is shown in Fig. 3.1. It includes “Charge Pump” block to serve as stimulus generator and “TDC” block to serve as response evaluator. To test a capacitive MEMS device, the MEMS structure is stimulated by DC current sources to its full operating range and then the associated DUT capacitor is measured to evaluate the response to the applied stimulus. The Charge Pump block comprises two external reference current sources that forms a charge pump and allows the scheme to perform charge-control tests on capacitive MEMS. The TDC block includes a comparator and a Time-to-Digital Converter. The test is performed in two phases to suppress the nonlinearity effects of the measurement circuitry. In the charging phase, the current source I_1 charge up the MEMS DUT capacitor until it exceeds a reference voltage, where the stop signal is generated. The time interval between the start and stop signals is measured by a TDC to determine the capacitor value. At the second

phase, the capacitor is discharged by I_2, and similarly the required time is measured by the TDC. This method is similar to the dual-slope measurement method widely used in industry standard products. For $I_1 = I_2$ in an ideal case the charge and discharge time intervals are equal however in practice due to noise and nonlinearities there is a difference between them.

The employed dual-slope measurement technique cancels out the effects of nonlinearities to the first degree increasing the measurement accuracy; this level of accuracy cannot be achieved by a single phase measurement system. Moreover, as shown in Figure 3.2, a reference capacitor is added to the proposed readout and BIST circuitry. The addition of a reference capacitor minimizes the noise effect and the nonlinearities associated within the readout circuit. It also minimizes the undesired effect of the parasitic capacitance.

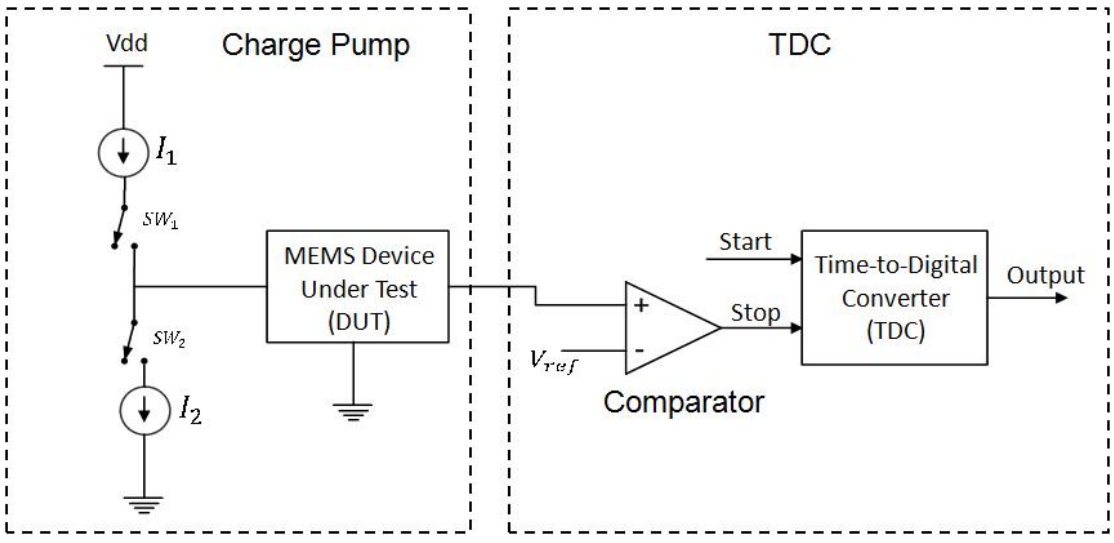


Figure 3.1: Simplified Block Diagram of the BIST Architecture

3.1.1 Charge Pump Block

The schematic diagram of the proposed circuit is shown in Figure 3.2. A reference capacitor which is equal to the MEMS capacitor in the free standing state is included in

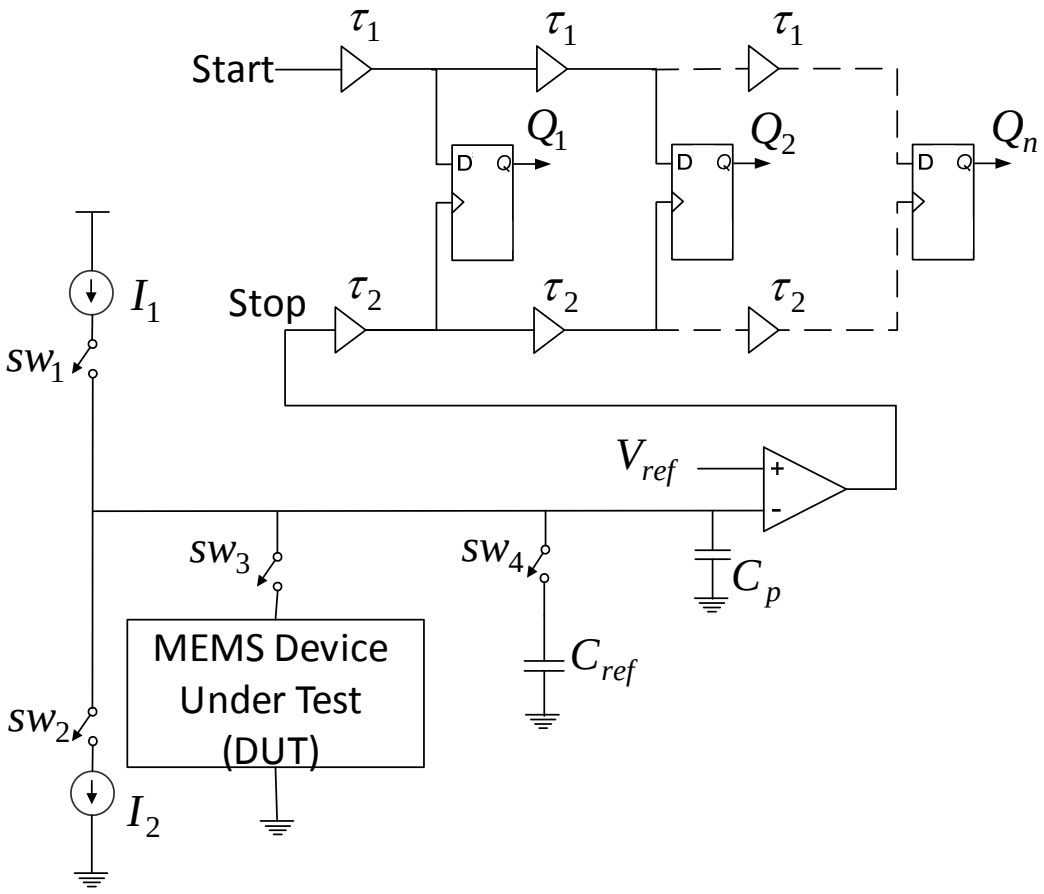


Figure 3.2: Schematic Diagram of the BIST circuitry

the circuit. The BIST scheme operates as follows. Initially, all the switches SW_1, SW_2, SW_3 and SW_4 are open. First SW_1 turns on and the reference current I_1 flows in the circuit. The time t_0 required to charge the parasitic capacitance C_p is measured. Next SW_4 is turned on connecting C_{ref} to the circuit. The required time t_1 to charge up

$C_{ref} + C_p$ is measured. The required time t_2 to charge C_{MEMS} is determined, where SW_3 is closed and SW_4 is disconnected.

3.1.2 Time-to-Digital Converter (TDC)

Figure 3.3 shows the basic circuit model for the Time-to-Digital converter (TDC) designed with a single delay line including identical delay cells. The delay between the rising edges of the start and stop signal are measured by the input of the controlled delayed flip-flops.

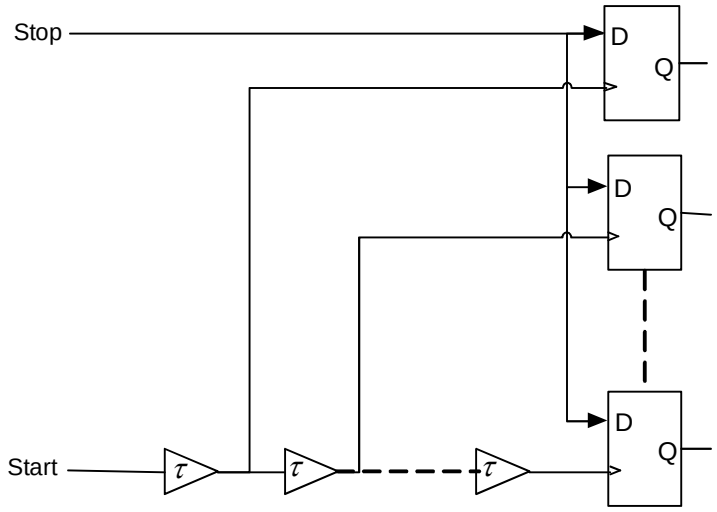


Figure 3.3: Basic time-to-digital converter using delay line

The flip-flops are triggered through multi-phase clock provided to the delay line by the applied start pulse and the number of toggled flip-flops determines the input time interval. The delay time of one single cell limits the measurement resolution in this scheme. However, we can design a Vernier Delay Line (VDL) using two delay lines for higher measurement resolution. The architecture of VDL is designed in such a way, that the delay lines produce multi-phase input signals and the flip-flops in the design act as an

arbiter to judge and compare the input signal phases and quantize the time intervals. The delay time of a delay cell in the upper delay line (τ_1) is slightly greater than that of the lower delay line (τ_2). With the START and STOP signals propagating in their respective delay lines, the time difference between the START and the STOP pulse is decreased in each Vernier stage by $\tau_d = \tau_1 - \tau_2$, which determines the achieved resolution. The STOP signal catches up with the START signal at position d_x in the delay line and gives information about the measured time t_x

$$d_x * \tau_d < t_x < (d_x + 1) * \tau_d \tag{3.1.1}$$

Since the delay difference between two delay elements determines the resolution, this difference can be made much shorter than the propagation delay of a single delay cell. In ideal case, the characteristic curve of TDC should have an identical quantization step size over the entire measurement range. But due to noise, mismatch and random variations of delay between delay cells or the physical length of the delay lines, in practice the quantization step varies over the input dynamic range. Thus the characteristic curve representing an actual TDC suffers from a non-uniform quantization step. Deviation of step size contributes to both Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) errors. We need a proper calibration of the TDC to suppress the effect of these nonlinearities effectively.

3.2 Measurement Principle and Mathematical Model

The sensitivity of fault detection for capacitive MEMS lies in sub-fF range. To measure such slight variations with high resolution and accuracy, noise, nonlinearities and other source of measurement uncertainty have to be minimized. Using the self-calibration technique for TDC, as described in [23], the undesired effects can be reduced to a great extent by self-calibration and the measurement process justification is described below.

When SW_1 in Fig. 3.2 is closed, the reference current I_1 charges the parasitic capacitance C_p. If the time required to charge C_p is t_0 we can write:

$$I_1 * t_0 = C_p * V_{ref} \tag{3.2.1}$$

When SW_1 and SW_4 in Fig. 3.2 are closed and SW_3 is open, the reference current I_1 charges the reference capacitance $C_{ref} + C_p$. If the time required to charge $C_{ref} + C_p$ is t_1 we can write:

$$I_1 * t_1 = \left(C_{ref} + C_p\right) * V_{ref} \tag{3.2.2}$$

Where, I_1 is the constant current source and V_{ref} is the reference voltage. When SW_3 is closed and SW_4 is open the MEMS capacitor becomes connected to the circuit and charged. If the time required to charge $C_{MEMS} + C_p$ is t_2 we can write:

$$I_1 * t_2 = \left(C_{MEMS} + C_p\right) * V_{ref} \tag{3.2.3}$$

From (3.2.1), (3.2.2), and (3.2.3) we can write

$$\frac{t_1}{t_0} = K_1 = \frac{C_{ref}}{C_p} + 1 \tag{3.2.4}$$

$$\frac{t_2}{t_0} = K_2 = \frac{C_{MEMS}}{C_p} + 1 \tag{3.2.5}$$

Solving (3.2.4) and (3.2.5) for parasitic capacitance C_p yields to:

$$\frac{C_{MEMS}}{K_2 - 1} = \frac{C_{ref}}{K_1 - 1} \tag{3.2.6}$$

When a MEMS sensor is activated, its capacitance deviates from the reference value in the free standing state C_{ref}. Assuming the change is ΔC, that is $C_{MEMS} = C_{ref} + \Delta C$ and from (3.2.6) we can obtain:

$$\Delta C = \frac{K_2 - K_1}{K_1 - 1} * C_{ref} \tag{3.2.7}$$

It can be seen that the variation of capacitance ΔC is not a function of I_{ref} and V_{ref}, hence the measurement uncertainty due to variations of these factors is significantly reduced. Consequently, the undesired effects of process, supply voltage and temperature variations on the measurement results are minimized. Moreover, the results obtained by discharging the capacitors through the bottom current source I_2 can also be used to reduce the nonlinearity effects of the BIST scheme on the measurement results.

In the measurement analysis the non-ideality effects have not been taken into consideration. In practice the accuracy and the resolution of the measurement results are affected by these factors. Nonlinearity, channel length modulation, charge injection,

clock feedthrough and noise are among the main factors contributing to the measurement uncertainty. Although it is possible to reduce the undesired effects of these factors by proper circuit design techniques, in practice the minimum detectable MEMS capacitance variation $\Delta C_{\min}$ is limited by noise level. To estimate $\Delta C_{\min}$, it is assume that the non-ideality effects is dominated by the rms noise voltage $V_{n,rms}$ of active components across the MEMS capacitance. The total integrated noise power at the output node in figure 3.4 is given by:

$$P_{n,out} = \frac{kT}{C_{MEMS} + C_p} = \overline{V_{n,rms}^2} \tag{3.2.8}$$

Where k is the Boltzmann constant $1.38 \times 10^{-23} J/K$ and T is the absolute temperature in Kelvin.

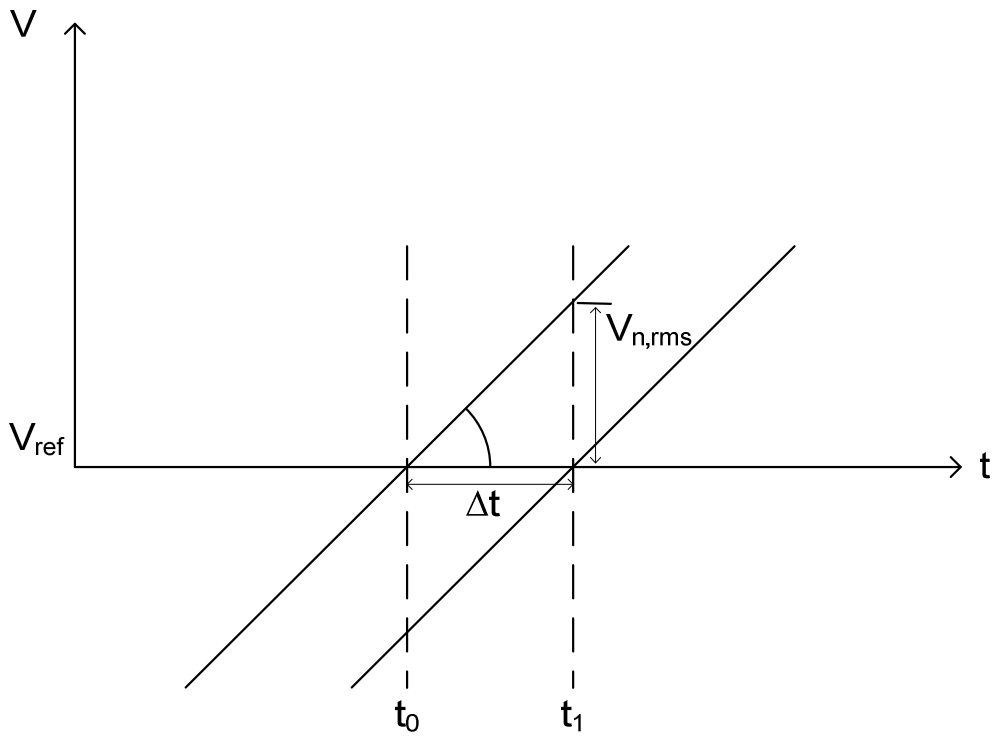


Figure 3.4: Timing error introduced due to thermal noise of active components

The timing error due to noise, as indicated in Figure 3.4, depends on the slope of transition and the rms noise voltage at the output. Assuming current source of *I*, the output slope is given by $\tan\alpha = I/C_{MEMS} + C_p$ and thus the timing error Δt_{rms} can be determined from:

$$\tan\alpha = \frac{I}{C_{MEMS} + C_p} = \frac{V_{n,rms}}{\Delta t_{rms}} \tag{3.2.9}$$

From (3.2.8) and (3.2.9) the minimum timing error Δt_{error} can be determined as $\Delta t_{error} = \sqrt{kT\left(C_{MEMS} + C_p\right)}/I$. The relation between variations of MEM capacitance ΔC_{MEMS} and time variation Δt can be expressed as $I \times \Delta t = V_{ref} \times \Delta C$. Since Δt has to be greater than or equal to Δt_{error}, the minimum detectable MEMS capacitance variation can be found from $I \times \Delta t_{error} = V_{ref} \times \Delta C_{\min}$ and can be written as:

$$\Delta C_{\min} = \frac{\sqrt{kT\left(C_{MEMS} + C_p\right)}}{V_{ref}} \tag{3.2.10}$$

Equation (3.2.10) indicates that the reference voltage has to be set to the highest value to ensure maximum measurement resolution. During the test phase, when a capacitive MEMS device is stimulated via electrical inputs, energy stored on the capacitor must be controlled to apply electrostatic force between the capacitor plates. This is established by one of following methods of (a) voltage-control and (b) charge control. Due to the ease of its implementation, the voltage control method is widely adopted [24] - [26].

Figure 3.5 shows a parallel plate spring-suspended MEMS capacitor C_{MEMS}. For voltage-control methods, if the distance between the plates is d, the electrostatic force F_e between the plates can be written as,

$$F_e = \frac{1}{2}\frac{C}{d}v^2 = \frac{\varepsilon A V^2}{2d^2} \tag{3.2.11}$$

The main disadvantage of the voltage-control methods is a strong dependency between the electrostatic force and the gap between the capacitor plates. This may lead to permanent damage due to the collapsing of the MEMS structure. In the proposed method using the charge-control, this dependency does not exist reducing the possibility of structural collapse in the test phase. If the total charge stored on the capacitor is Q and the distance between the capacitor plates is d, the stored energy W is equal to:

$$W = \frac{q^2 d}{2\varepsilon A} \tag{3.2.12}$$

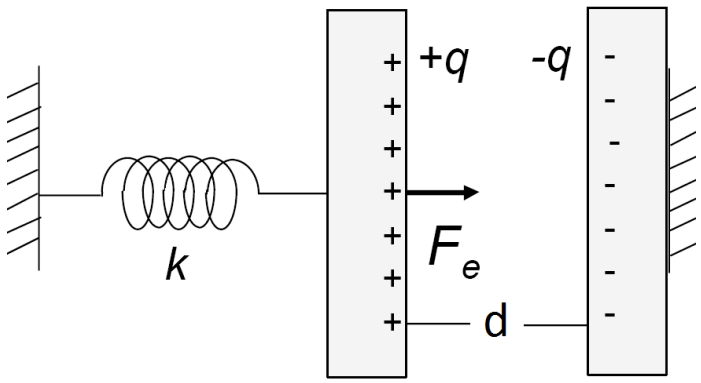


Figure 3.5: Spring-suspended model of capacitive MEMS devices

Where, ε is the permittivity and A is the plate area. The relationship between the electrostatic force F_e and the stored energy in charge-control method can be expressed as:

$$F_e = \frac{\partial W(Q,d)}{\partial d} = \frac{Q^2}{2\varepsilon A} \tag{3.2.13}$$

As observed from (3.2.13), the electrostatic force F_e does not depend on the gap between the plates any longer, minimizing the risk of MEMS structural collapse during the test phase. Figure 3.6 shows the relation between the electrostatic force in voltage and charge control techniques.

For the spring-suspended capacitor shown in Figure 3.4 the electrostatic force can also be written as,

$$F_e = kx \tag{3.2.14}$$

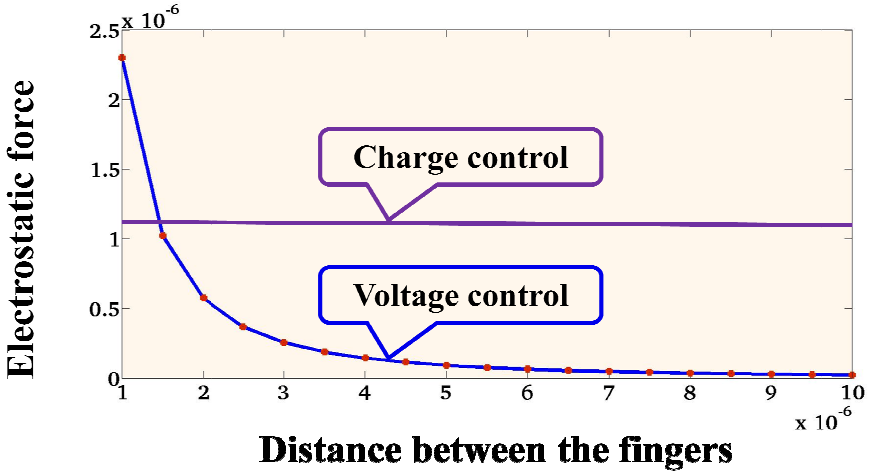


Figure 3.6: Electrostatic Force versus the Gap in Voltage-Control and Charge-Control Methods

Where k is the spring constant and x is the movement of the plate in either direction from the free standing state. Assuming the distance between the plates, d is changed from d_0 to $d_0 - x$ due to an applied electrostatic force where d_0 the free standing distance, we can find the following expression for d :

$$d = d_0 - x = d_0 - \frac{F_e}{k} = d_0 - \frac{Q^2}{2\varepsilon A k} \tag{3.2.15}$$

Using (3.2.15) and basic equation of charge $Q = CV$, we can obtain the expression for voltage across the plates:

$$V = \frac{Q}{C} = \frac{Q}{\varepsilon A}\left(d_0 - \frac{Q^2}{2\varepsilon A k}\right) = Q\left(\frac{d_0}{\varepsilon A} - \frac{Q^2}{2\varepsilon^2 A^2 k}\right) \tag{3.2.16}$$

So, equation (3.2.16) indicates that, as the gap between the plates decreases, the capacitor voltage also decreases. This is contradictory with the voltage-controlled methods where increase in voltage decreases the gap and eventually increasing the electrostatic force to collapse the MEMS structure.

3.3 Self-calibration of the BIST Scheme

Proper calibration is required for the proposed BIST circuitry to minimize the nonlinearity effects and to improve the measurement accuracy. It is shown mathematically in equation (3.2.7) that, the change in the components of the stimulus circuit has no impact on the measurement result and is mostly determined by the accuracy of TDC module in the TDC block. Hence, by calibrating the TDC properly, the measurement uncertainty can be greatly reduced. The calibration is done by constructing the characteristic curve representing the TDC. This is done by exciting the convertor with

a series of known time intervals to quantify the quantization steps representing the curve. The TDC measurement error is approximated from the characteristic curve and compensated.

Different TDC calibration methods described in literature [11], [23] can be adopted, but the majority of them require precise and expensive external instruments to perform the calibration. However, when the TDC consist of Vernier delay lines, the calibration can be carried out through statistical methods without requiring the need for costly external equipment [24]. For the calibration of the proposed BIST circuitry, to the technique presented in [23] was employed. As shown in Figure 3.7, by configuring the delay lines in the proposed TDC as ring oscillators, a set of time intervals are generated with identical probabilities of events. These time events are then applied as input stimuli to determine the TDC characteristic curve from the responses of these time events. To produce proper time events for the TDC calibration and to reduce the overall delay difference between the two delay lines additional delay cells to the feedback path of the faster delay line are added. Upon activation of the feedback paths, the ring oscillators start operating at close frequencies and generate evenly spread time events. If T_1 and T_2 are the periods, n is the number of delay cells in each delay line and τ_1 and τ_1 represent one-cell delay in the delay lines respectively in Figure 3.6, the frequencies can be obtained as:

$$f_1 = \frac{1}{T_1} = \frac{1}{2 \times n \times \tau_1} \tag{3.3.1}$$

$$f_2 = \frac{1}{T_2} = \frac{1}{2 \times n \times \tau_2} \tag{3.3.2}$$

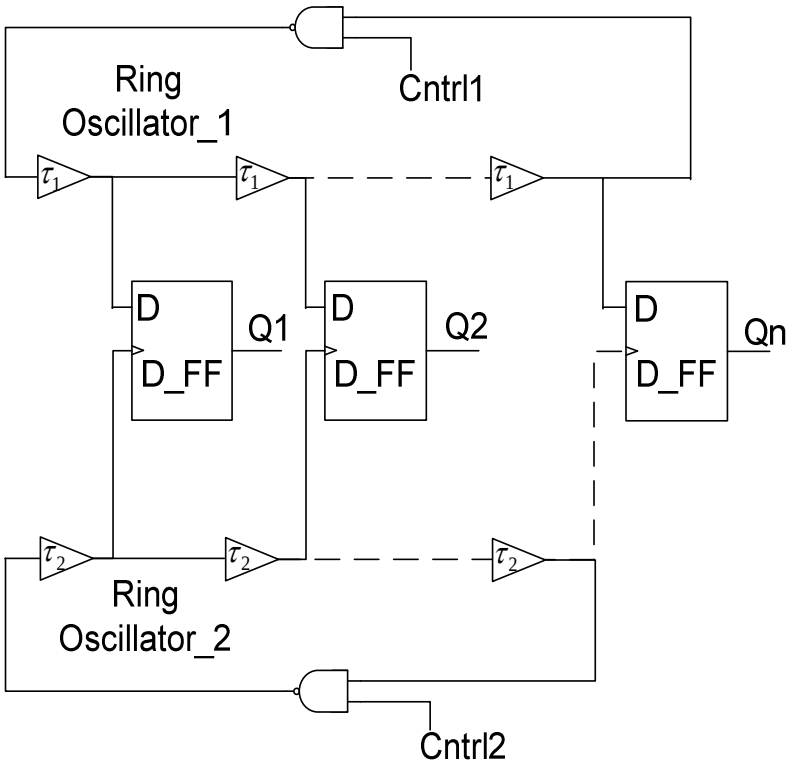


Figure 3.7: Delay lines configured as ring oscillators to generate time events for the TDC calibration

CHAPTER IV

DUT FABRICATION AND ANALYSIS OF SIMULATION RESULTS

To evaluate the performance of the proposed BIST and readout circuitry, a MEMS comb drive actuator was designed as a Device Under Test (DUT) using the Intellisuite CAD tools. The BIST circuitry was implemented using Cadence design tools. Common fabrication faults were then injected into the DUT and the variation in capacitance is measured through a readout circuit.

4.1 MEMS Comb Drive (DUT)

The designed comb drive had eight fingers with a structural layer made of poly-silicon. The structure has 4 movable fingers connected to a movable arm, and 4 fixed fingers attached to the substrate by anchors. This layout is similar to the ADXL series accelerometers concept developed by Analog Devices Inc. [3], [27]. Figure 4.1 shows the

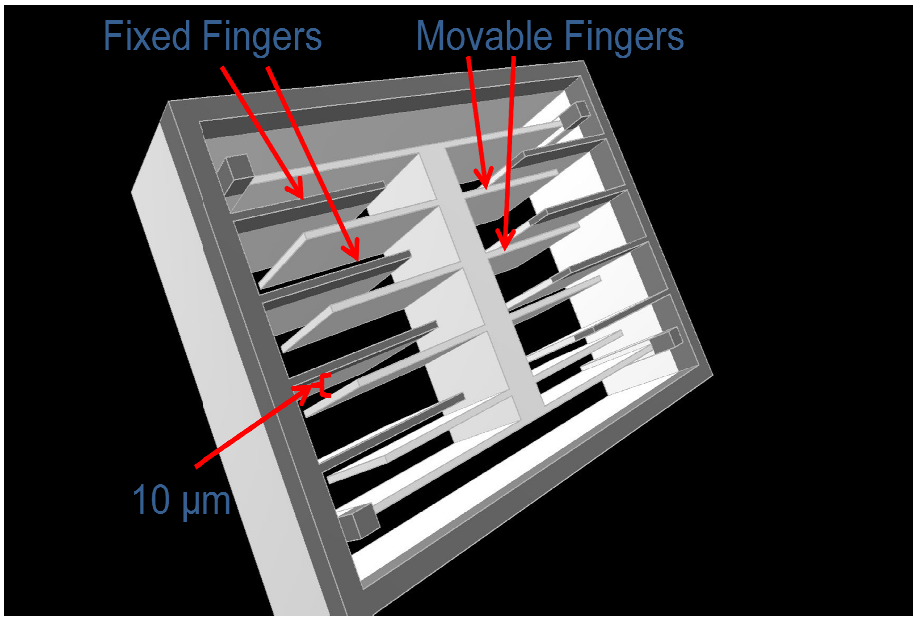


Figure 4.1: Designed comb drive used as a DUT

designed fault-free comb drive in steady state where no electrical or mechanical forces are applied to the structure. However, the comb drive capacitance is gradually charged up during the test phase due to the input current stimulus. As a result, an electrostatic force is formed between the fingers and subsequently displaces the movable arm. The entire process changes the overall capacitance and figure 4.2 shows the characteristic curve for such DUT. It can be seen that the capacitance varies from a minimum of 65.36 fF at the

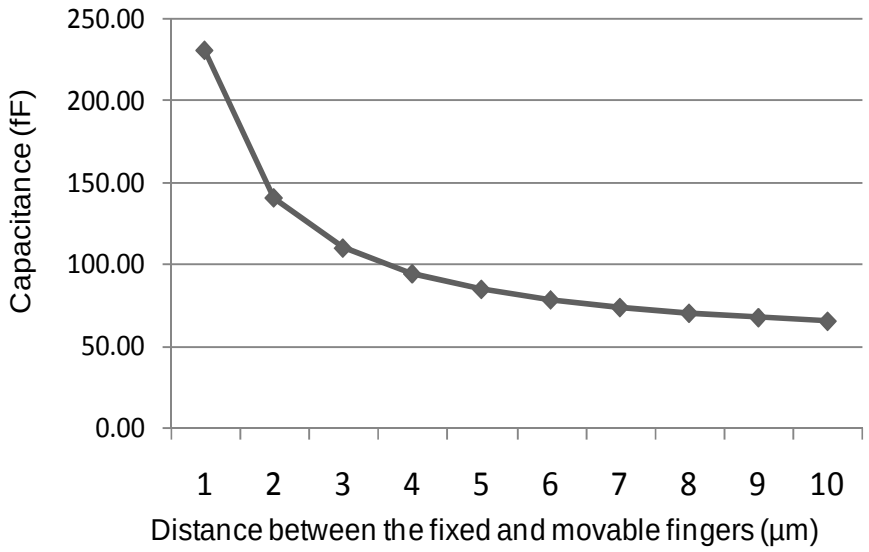


Figure 4.2: Characteristic curve of the MEMS structure used as a DUT

free standing state to a maximum of 230.4 fF at the full dynamic range. The nonlinearity between the variation of the capacitance and the distance can be attributed to the effects of side walls and fringing capacitances.

Then some common catastrophic and parametric fabrication faults were injected into the designed DUT to see the capacitance variation. The faults are: a) missing finger, b) finger height mismatch, and c) etch variation as shown in Figure 4.3. Table I shows the capacitance change for different etch variation in different directions. Figure 4.4 shows

the simulation result of the DUT with one missing finger and its effect on the overall capacitance of the DUT. The minimum variation of capacitance from nominal value is 3.5 fF as shown in figure 4.4.

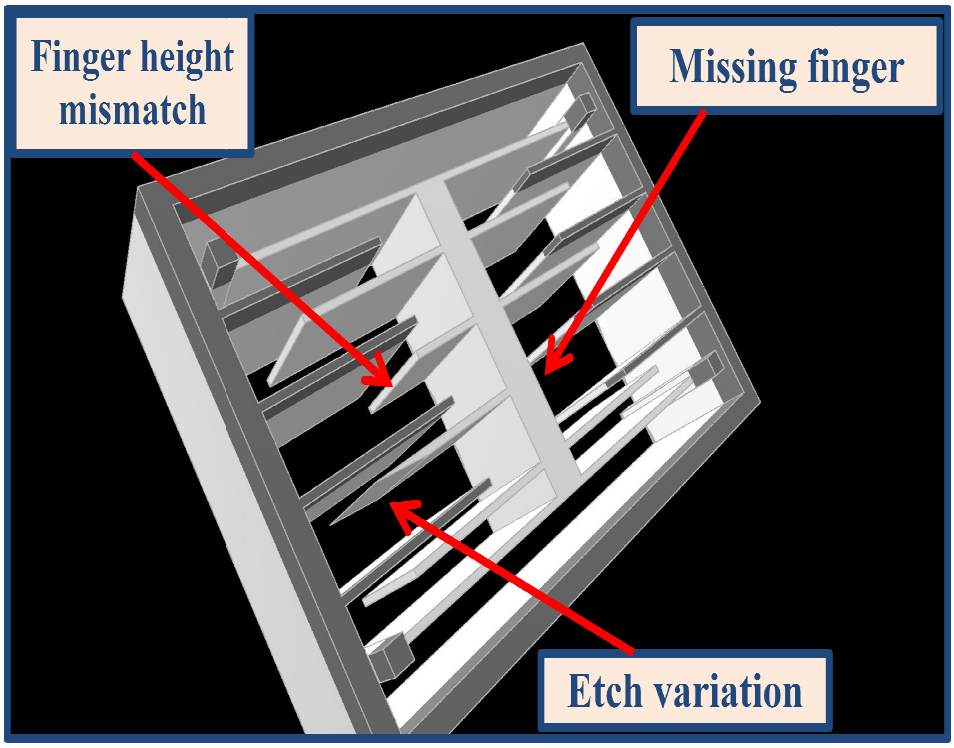


Figure 4.3: Common fabrication faults injected in the DUT

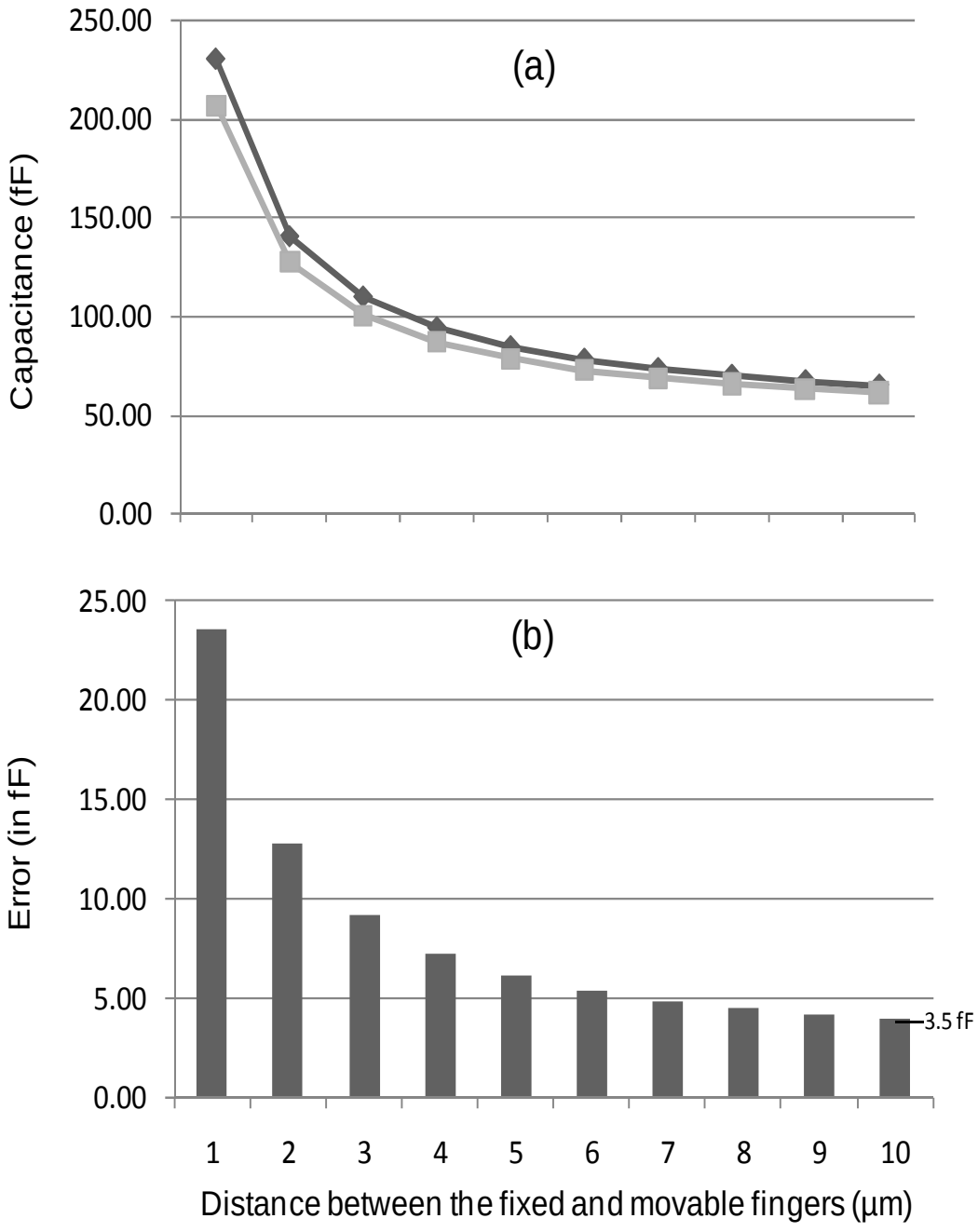


Fig. 4.4: The effect of a broken finger on the characteristic curve.

TABLE I: EFFECT OF ETCH VARIATIONS IN DIFFERENT DIMENSIONS ON MEASURED CAPACITANCE

Etch Variation (µm)	**X - Direction**		**Y - Direction**		**Z - Direction**	
	Depth (µm)	Measured Capacitance (fF)	Depth (µm)	Measured Capacitance (fF)	Depth (µm)	Measured Capacitance (fF)
Defect-Free	65.00	65.36	10.0	65.36	40	65.36
1%	64.35	65.11	9.9	65.55	39.6	64.89
2%	63.7	64.86	9.8	65.75	39.2	64.43
5%	61.75	64.09	9.5	66.35	38	63.03
10%	58.5	62.81	9.0	67.52	36	60.07

4.2 Test circuitry and TDC schematic

The test circuitry was designed using CADENCE environment in tsmc65nm technology. As shown in figure 4.5, a library capacitor named "*moscap_rf*" is used for both the MEMS and reference variable capacitors. The CNT pin controls the operational modes of the circuit. When CNT is high, the circuit operates in the normal mode and START and STOP signals are generated. The STOP signal is generated by charging the MEMS capacitor with a delay ΔT equals to the charging time of the capacitor. The STOP and START signal are fed into the TDC circuit where the stop signal operates as the clock signal for the D-flip-flops in the TDC circuit. Two buffers to sharpen the signal are

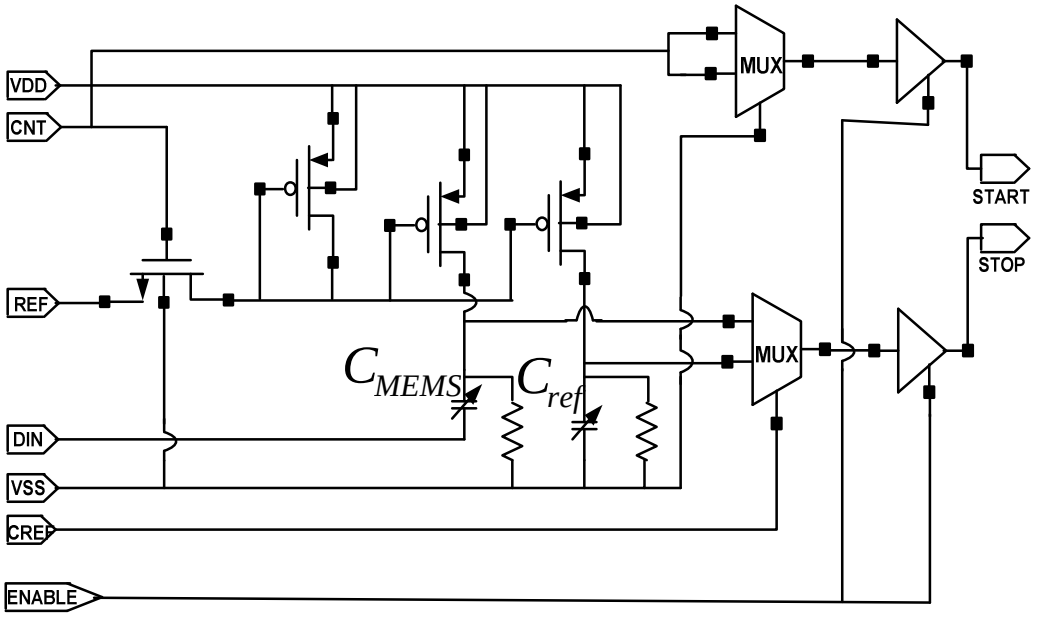


Figure 4.5: Schematic view of charge pump block consisting of MEMS and reference capacitors

inserted before the STOP and START signals. The current is controlled by an external resistor through the REF pin. The CREF input selects between the outputs of MEMS and reference capacitors through the bottom MUX. The ENABLE pin is used to introduce self-test for TDC which controls the propagation of STOP and START signals to TDC. When ENABLE is set low the outputs from generation circuitry are not propagated through the tri-state buffer used and STOP and START pins become input pin to test the TDC.

The TDC consists of 32 blocks as shown in figure 4.6. Each block consists of 32 single delay elements to provide higher dynamic range in terms of detecting the time variation. Vernier delay line is formed using D-flip-flop's and MUX's. The resolution is set by the response delay of the MUX as shown in figure 4.7. After each stage, the delay

difference between the stop and start signal decreases. When the delay is zero, a transition in the D-flip-flops output is set indicating the charging time of the capacitor. In the readout mode, CNT is set to low and the DIN pin is stimulated with clock pulses to extract the transition states of the d-flip-flop. However the DIN pin also controls the variable MEMS capacitor by applying an external voltage and changing the capacitance accordingly. Figure 4.8 shows the relationship between time variation Δt in comparison to capacitance variation ΔC. The relationship is almost linear as shown in figure 4.8.

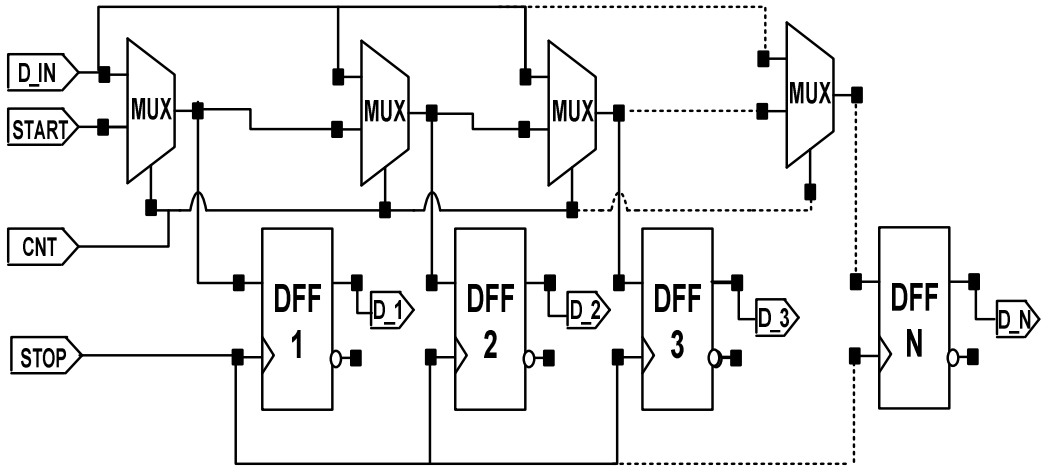


Figure 4.6: Employed TDC where delay lines configured as ring oscillators to generate time events for the self calibration

4.3 Schematic level simulation results

Using Cadence design tool the test circuitry, charge pump block was implemented in schematic level and simulations were performed to see the generation of START and STOP signals as defined earlier. Please see figure 4.9. The delay is due to the charging time of the MESMS capacitance.

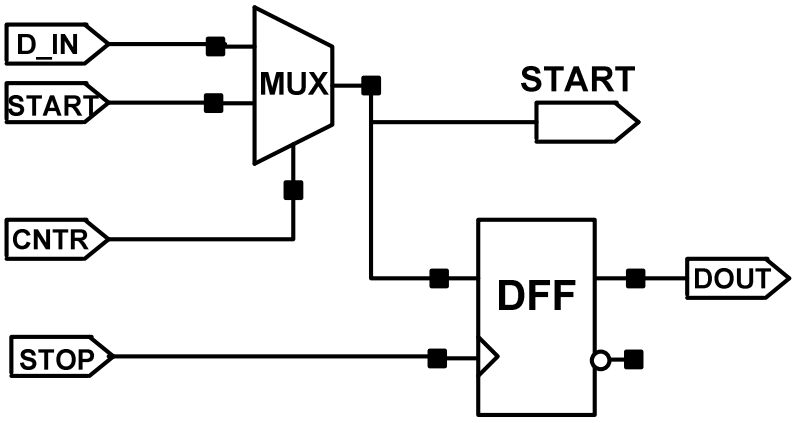


Figure 4.7: The schematic of each delay block

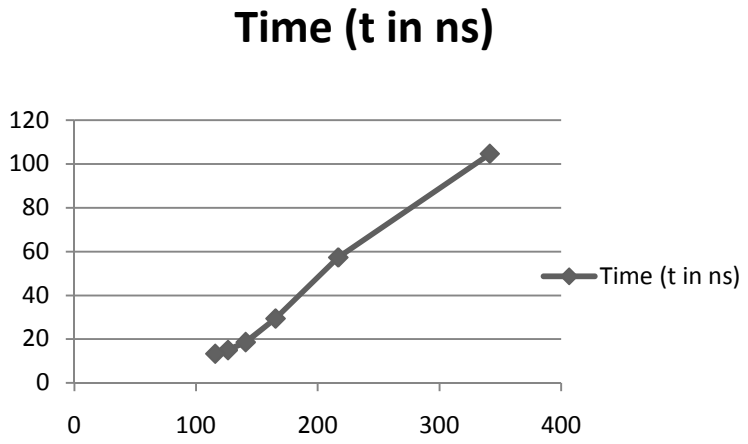


Figure 4.8: Relationship between capacitance variation and converted time variation

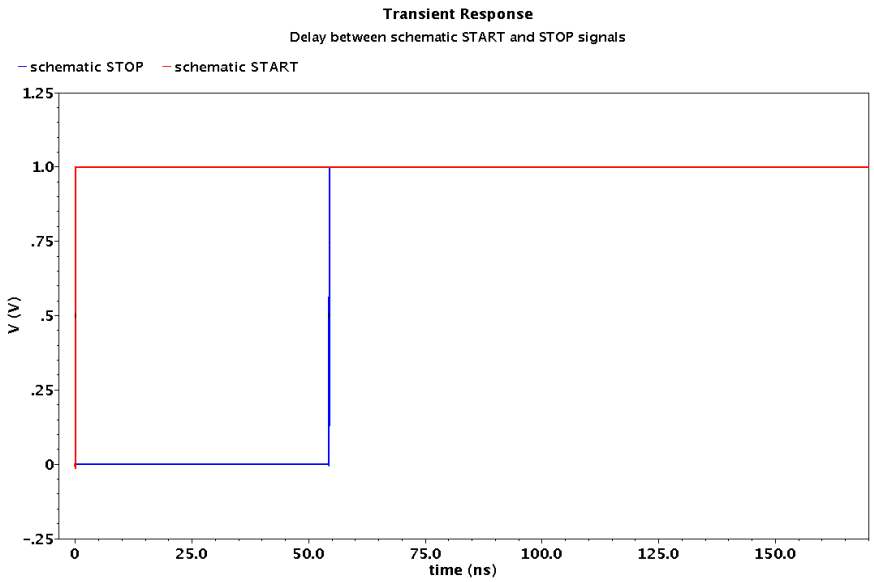


Figure 4.9: Successful generation of START and STOP signals in schematic level

The TDC block was also implemented in schematic level and simulated with two deferent delays between START and STOP signals. Figure 4.10 and figure 4.11 shows the detection of this delay in D-Flip-Flops output. First case the delay between START and STOP signal was set to 750 ps, and second case the delay was 900 ps. From the pre-layout simulations it is evident that the TDC is working fine in schematic level to detect the transition for a given delay between START and STOP signals. The average delay between the top and bottom delay lines can be approximated to 30 ps in each vernier stage. With careful measurement it can be found that the MUX in top line adds about 26 ps delay and the D-flip flop has its own delay of around 4 ps to be added to the top delay line. In each vernier stage the STOP signal overcomes 30 ps delay and eventually catches up the START signal in corresponding flip-flop number where it sees a transition.

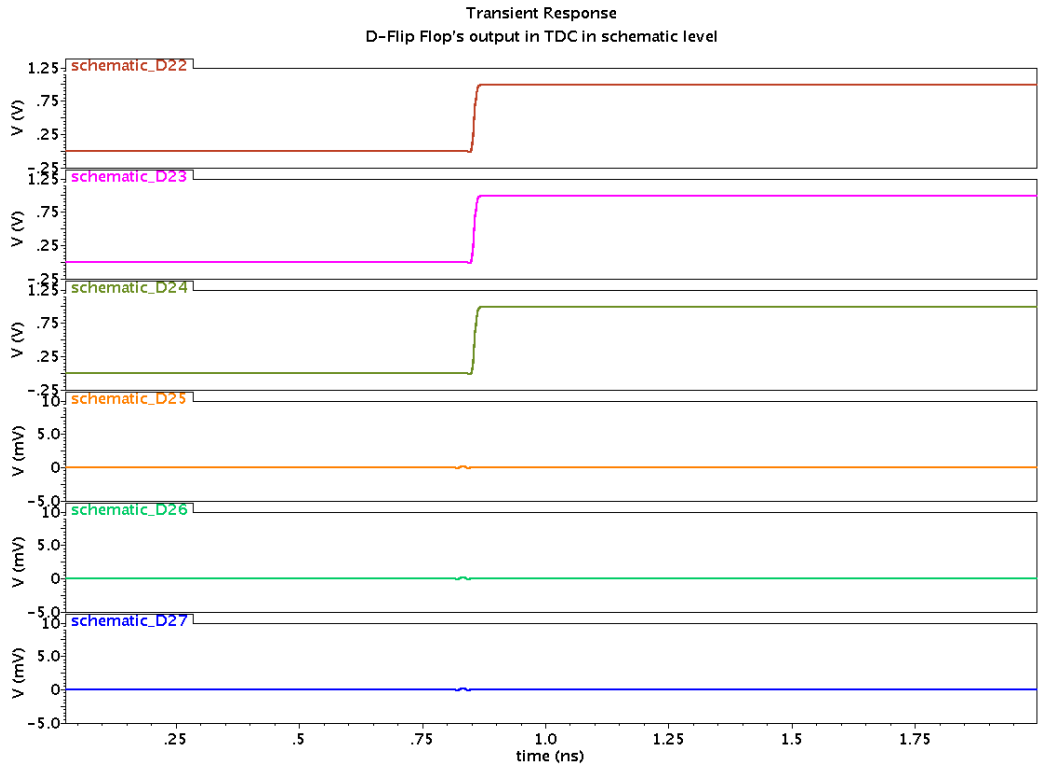


Figure 4.10: Transition between flip flop 24 and 25 in TDC vernier delay line for schematic level simulation while delay between start and stop is = 750 ps

4.4 Layout and fabrication of the proposed chip and post layout simulation

The proposed schematic is designed using tsmc65nm technology for fabrication. A CADENCE design tool was used for this purpose. Appendix describes the fabrication process elaborately. The tsmc65nm technology is a new technology adopted by Canadian Microelectronic Corporation (CMC). Initially it seemed very hard to understand with the limited number of resources supplied by CMC along with the kit. However, the CMC fabrication team was very much supportive and provided with all the information needed to complete the fabrication. This technology also provided the auto routing tool which proved very helpful while designing the chip. At first the layout of Time-to-Digital

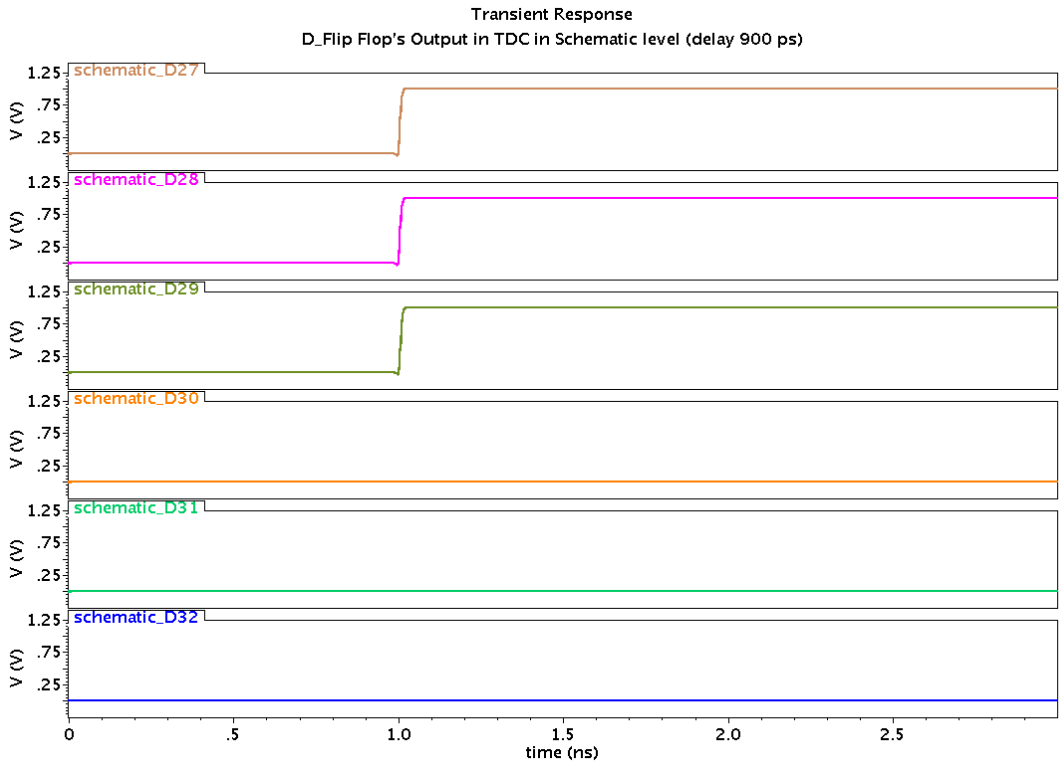


Figure 4.11: Transition between flip flop 29 and 30 in TDC vernier delay line for schematic level simulation while delay between start and stop is = 900 ps

Converter (TDC) single cell was extracted, and tested for correct functioning. Figure 4.12 shows the layout view of TDC single cell that was the base for final TDC. However, our TDC final block consisted of 32 such TDC single cells and the layout was also extracted accordingly. Simulation results confirmed the TDC is working properly with given START and STOP inputs. Figure 4.13 shows the final layout view of full TDC block.

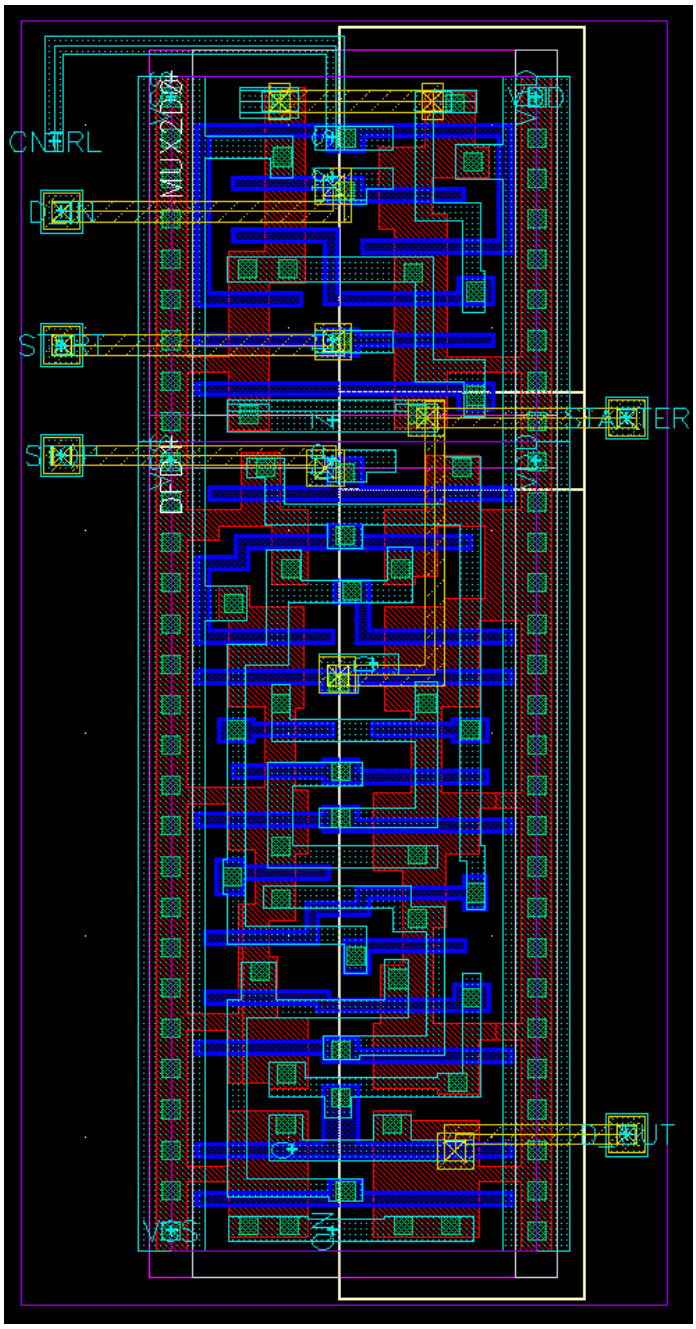


Figure 4.12: Layout view of TDC single cell consisting of a MUX and one D-Flip-Flop

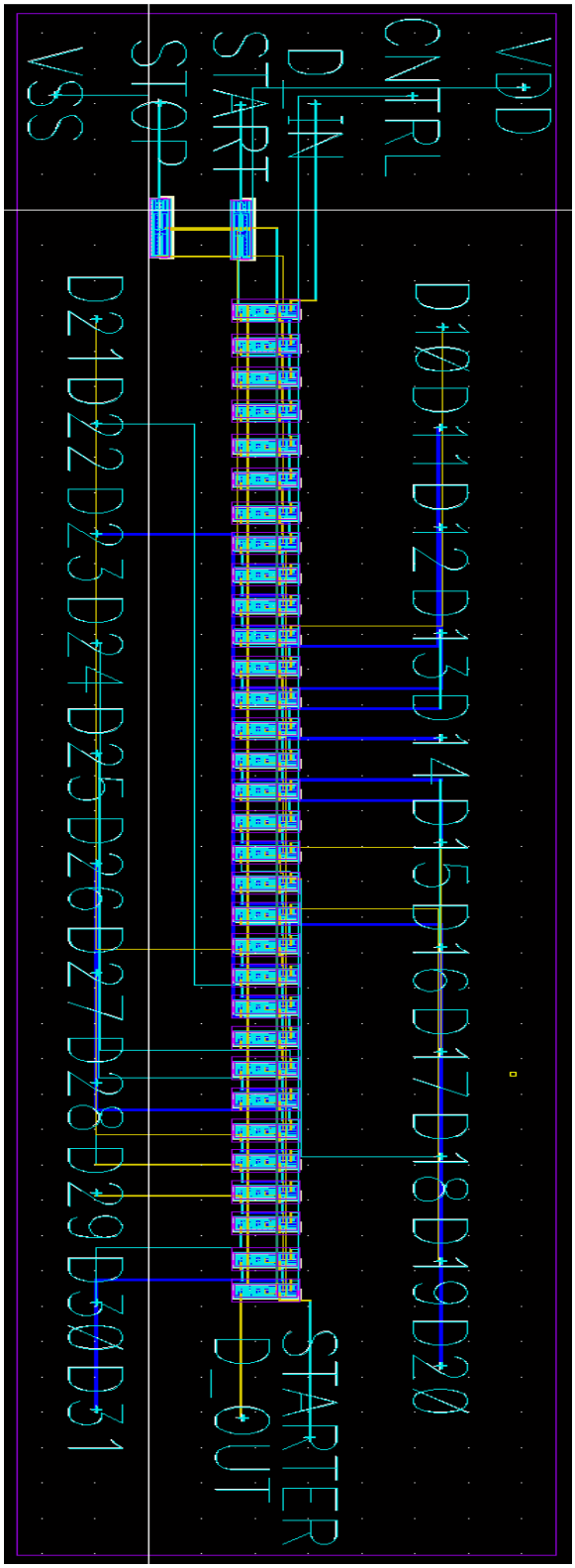


Figure 4.13: Final layout view of TDC block consisting of 32 TDC single cells

Then the test circuitry for generation of START and STOP signal was extracted for layout and simulated to see if the circuitry is functioning properly or not. Figure 4.14 shows the layout view of charge pump block with dimension $73.1\ \mu m \times 73.7\ \mu m$. Figure 4.15 shows the complete chip that was sent for fabrication. The total dimension for the chip is $643.6\ \mu m \times 996\ \mu m$.

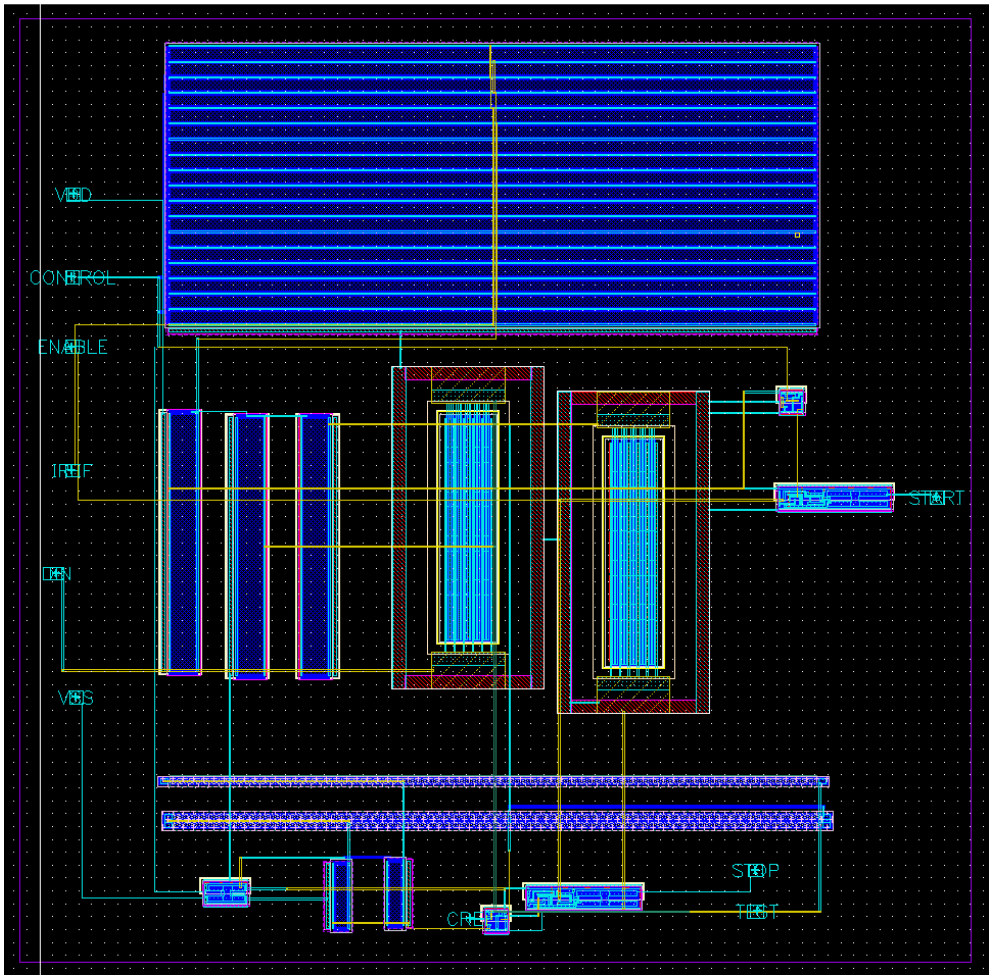


Figure 4.14: Complete layout view of charge pump block. START and STOP pins are input/output pins

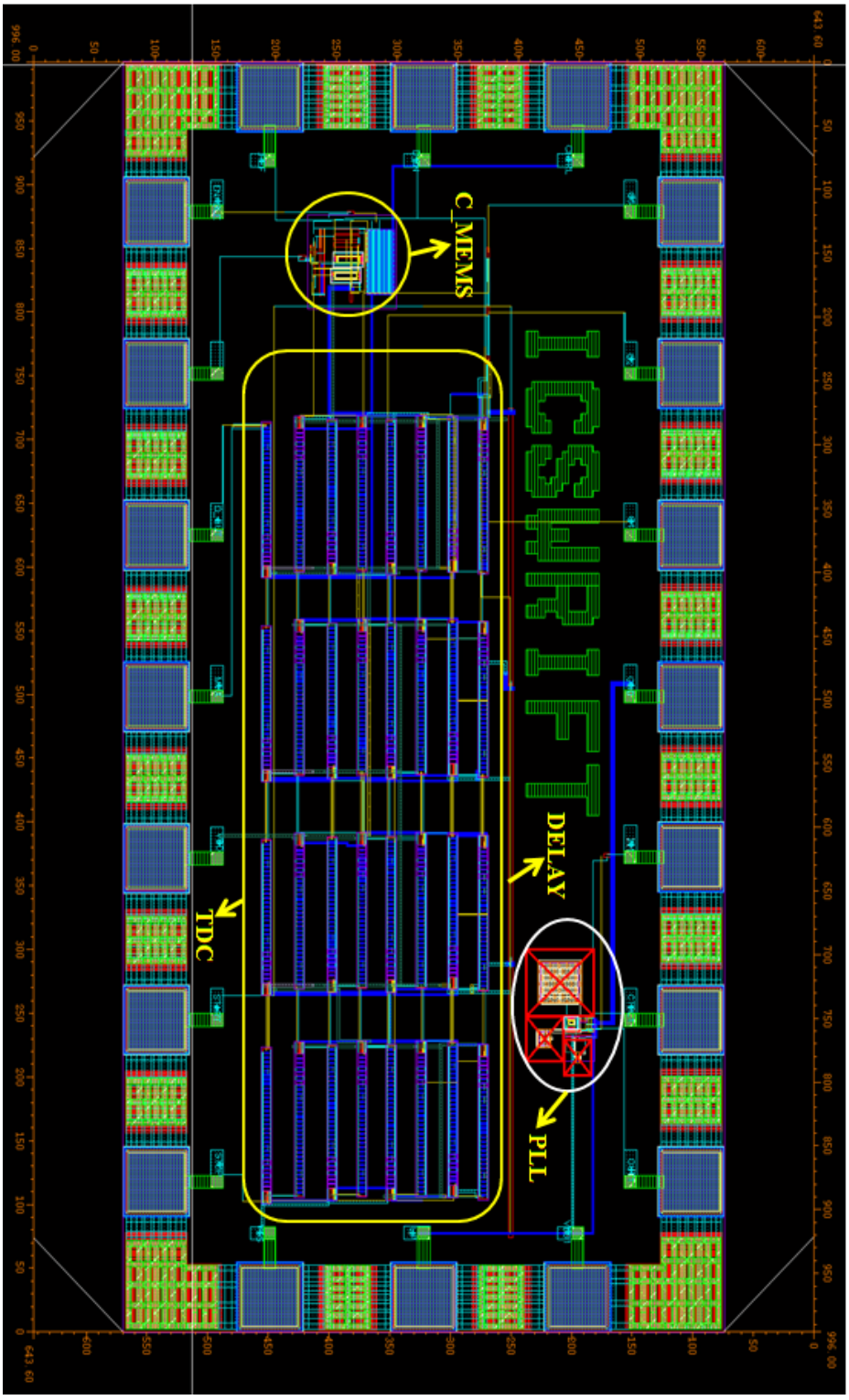


Figure 4.15: Layout view of the complete chip

The full layout design for the proposed chip is then verified through Design Rule Check (DRC) and Layout VS Schematic (LVS). Finally post layout view was extracted and simulations were performed to compare with the schematic level results. MEMS capacitance block was separately extracted in post layout view and figure 4.16 shows the successful generation of START and STOP signal in calibre view. The TDC was also extracted separately for simulation purpose and figure 4.17 and 4.18 shows the detection of capacitance variation for two different delays as in schematic level. It is seen the measurement delay in post layout view is higher than the schematic level and the detection takes place in earlier stages of D-Flip-Flops.

As discussed previously, the delay between the START and STOP signals in figure 4.16 is due to the charging time of the MEMS capacitor. This delay is then detected by the TDC using Vernier delay line. As the STOP and START signal propagate

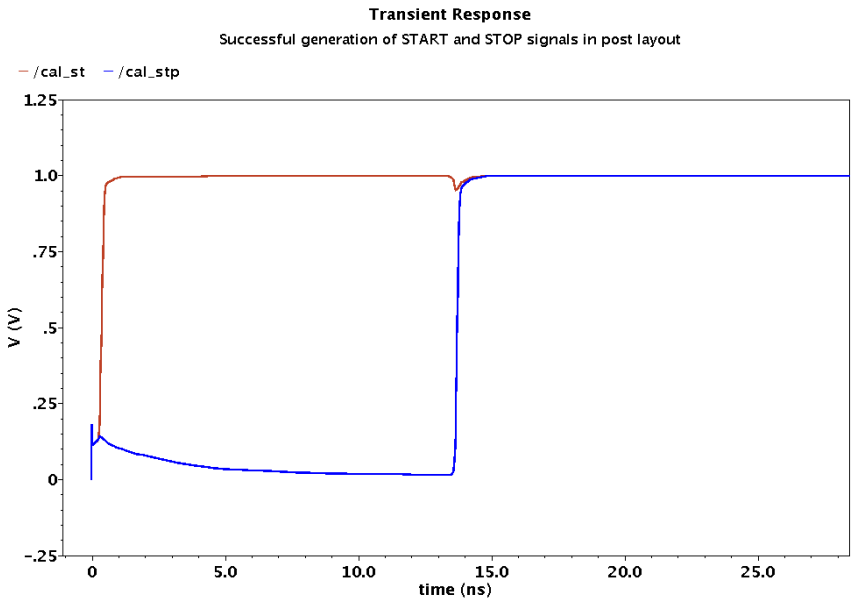


Figure 4.16: Successful generation of START and STOP signals in MEMS capacitance block when an external current source is supplied

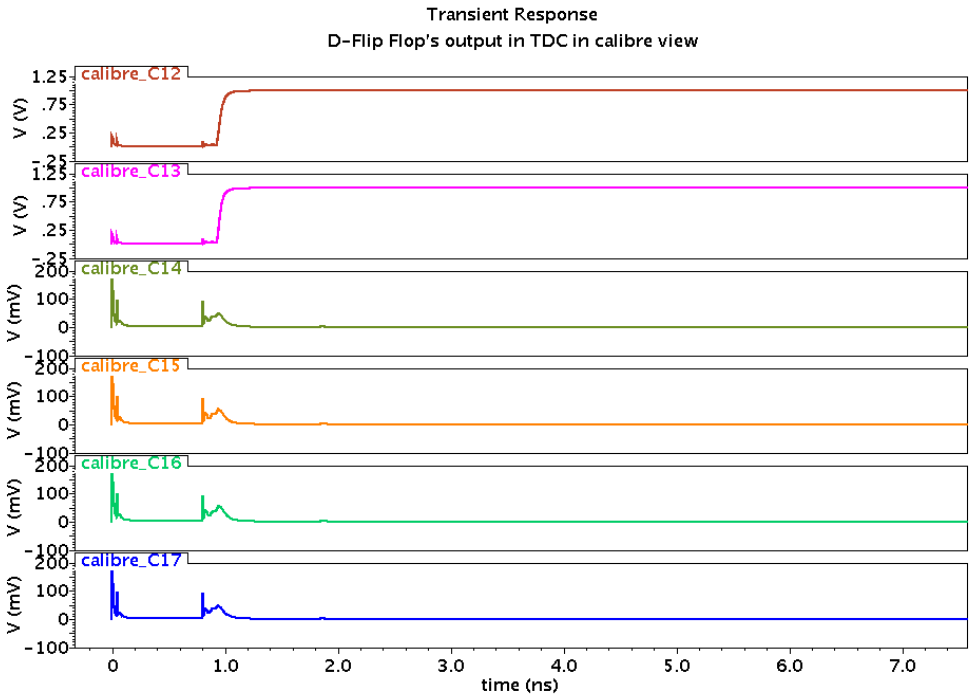


Figure 4.17: Transition between flip flop 13 and 14 in TDC vernier delay line for post layout caliber view simulation while delay between START and STOP is = 750 ps

in the TDC block, the delay between the signals decreases. When the delay reaches zero, a transition in the d-flip-flop is set indicating the time required to charge the MEMS DUT as shown in figure 4.17 and figure 4.18. The difference in detecting the D-Flip-Flop transition between the schematic and post layout design is because the resolution set by the delay has been altered and the resolution of the TDC is set by the delay difference between the top and the bottom lines. In schematic level it is measured to be ≈ 30 ps and in post layout design ≈ 50 ps. This variation in vernier delay lines is due to the added parasitic capacitance and resistance of the metal lines that are taken into consideration when extracting the parameters for the layout simulation. Table II shows the relative detection of capacitance variation in schematic and post layout simulation. The difference in each stage is ≈ 20 ps.

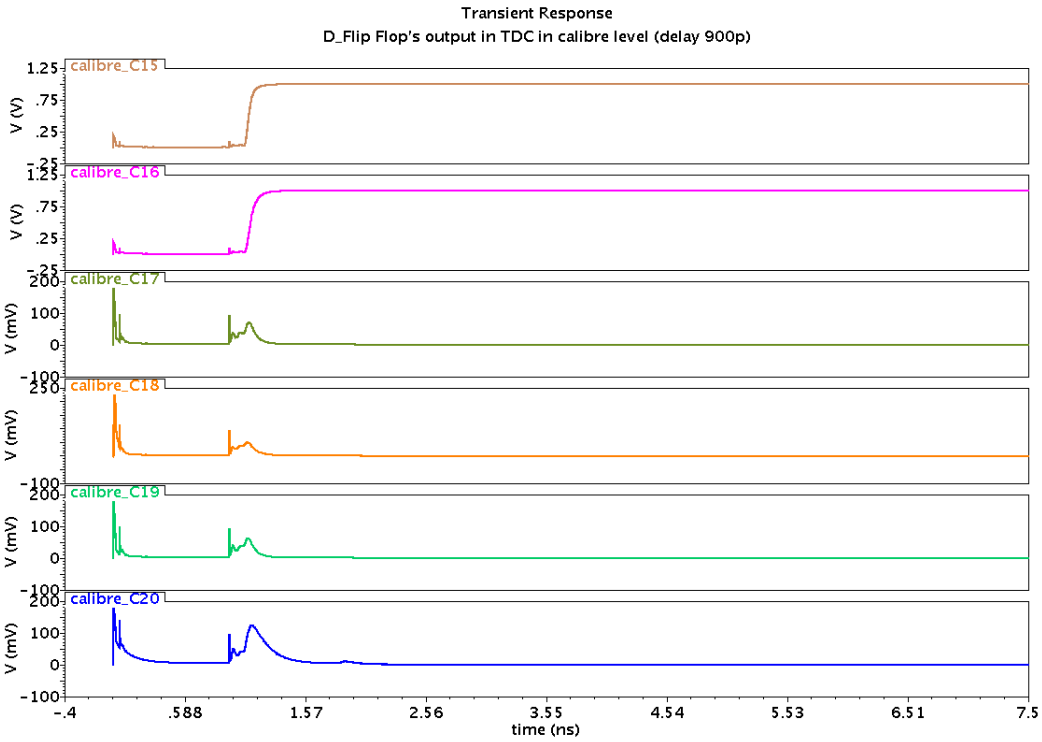


Figure 4.18: Transition between flip flop 16 and 17 in TDC vernier delay line for post layout caliber view simulation while delay between START and STOP is = 900 ps

4.5 Fabricated chip and measurement results

The chip was designed via Canadian Microelectronic Corporation (CMC) and was sent back to the lab by mid-July. Figure 4.19 shows the microscopic picture of the actual fabricated chip. Some basic testing has been performed with available instruments which showed promising results. Figure 4.20 shows the test setup with basic signal generator and oscilloscope. According the working principle, when CNT is high, we should expect it to be propagated to the START pin. At the same time, if reference current is supplied the MEMS capacitor should charge to VDD and show up in the STOP pin, providing the ENABLE pin is high. Figure 4.21 shows the measured START and STOP signal.

)UT SIMULATION

s	Added delay in pico-seconds per stage
	20
	20
	20
	20
	20

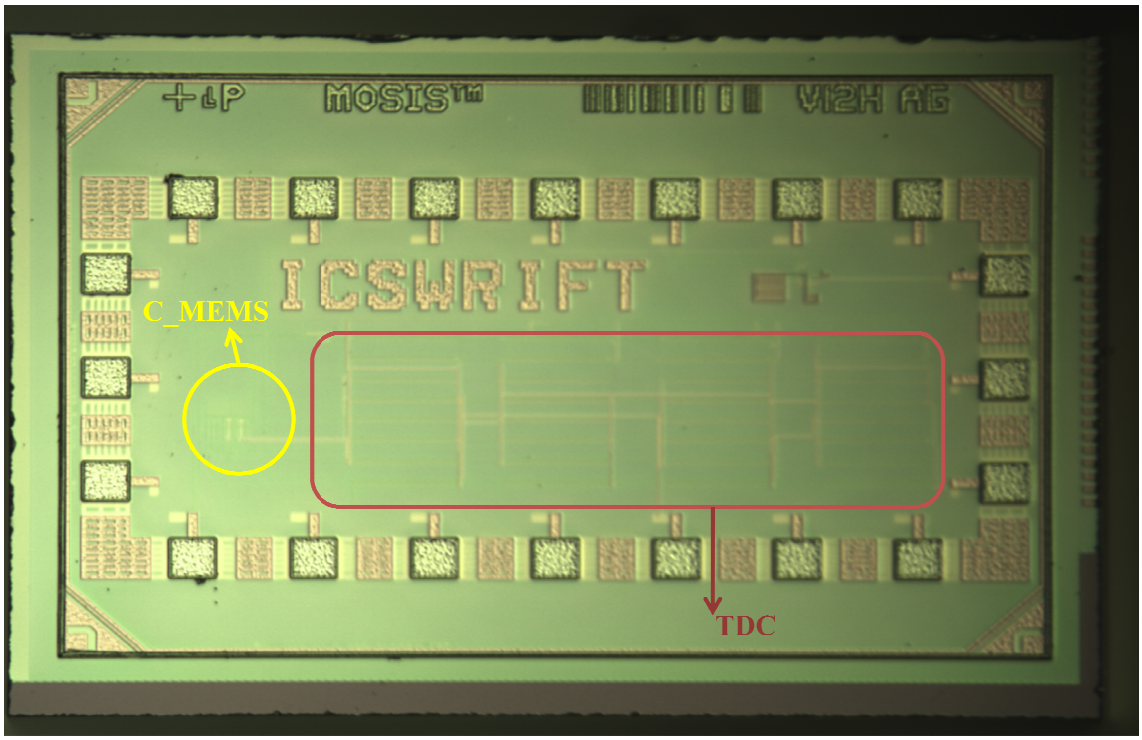


Figure 4.19: Microscopic view of the fabricated chip

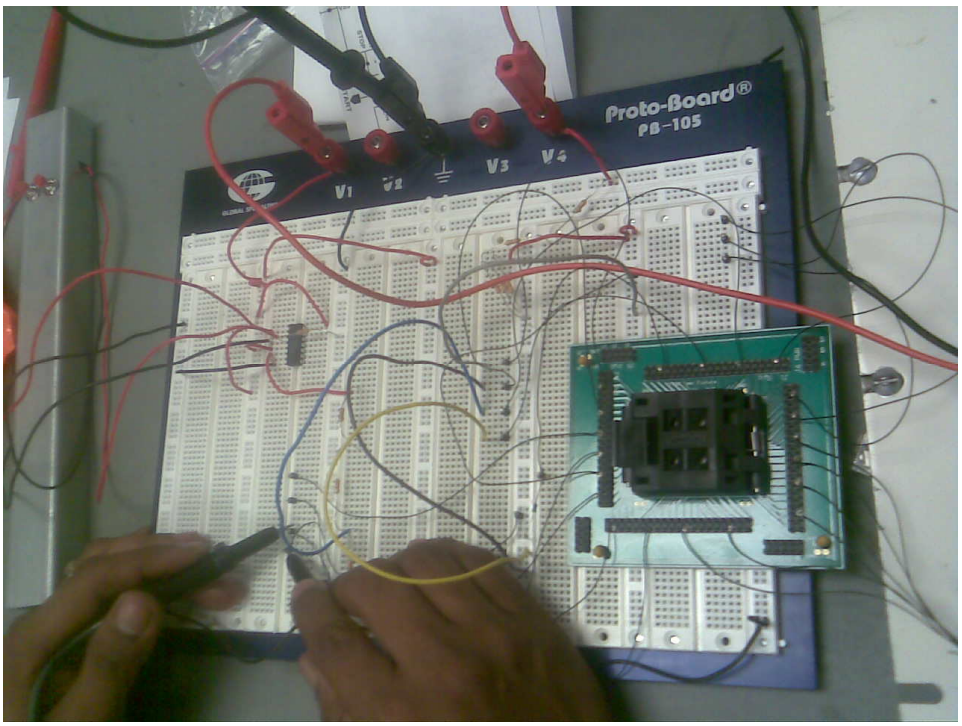


Figure 4.20: Test setup for the fabricated IC

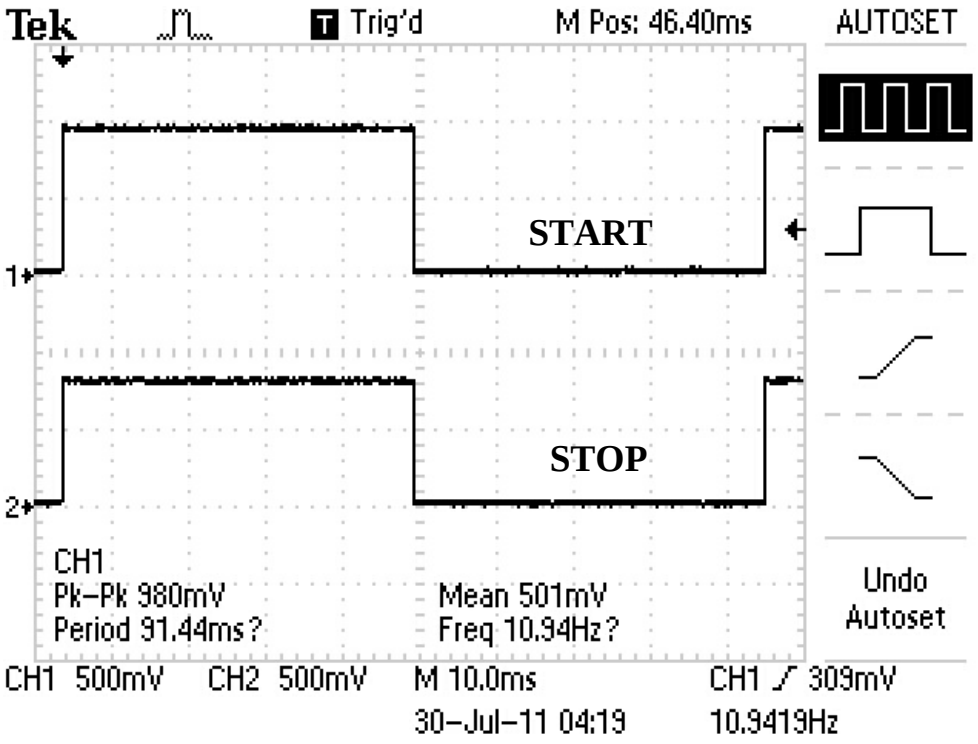


Figure 4.21: Measured START and STOP signal

The delay between START and STOP as expected is in the range of nanosecond. Such a short time interval can better be shown if an oscilloscope with a higher measurement resolution is used. To test the TDC the ENABLE pin was set to LOW, so that the START and STOP signals did not propagate from stimulus generator. The TDC was tested separately, a clock signal generated by a signal generator was used to drive STOP signal. The TDC output logic is a function of the START signal, for a HIGH input all TDC outputs are expected to be HIGH and for a LOW input the outputs have to be LOW. The TDC function was properly tested and the measurement results met the expectations. Figure 4.22 shows the measured TDC's outputs (DOUT and Q1) when the START signal is set to HIGH.

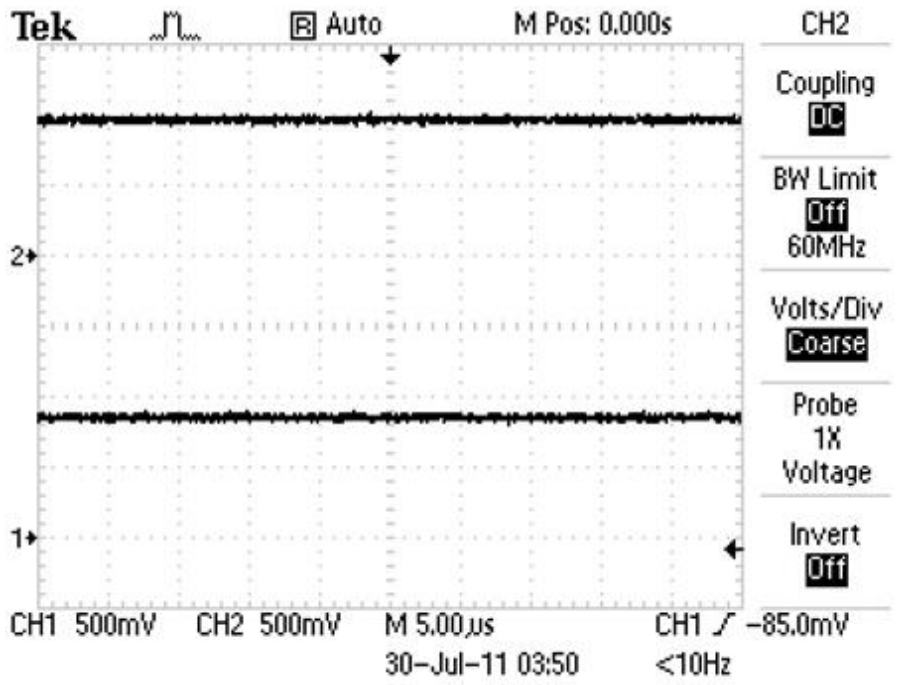


Figure 4.22: HIGH at DOUT pin and Q1 pin when START signal is HIGH

Then an advanced oscilloscope was used to measure the delay between START and STOP signals. This oscilloscope TDS 8000 was provided by CMC. Figure 4.23 shows the delay between measured START and STOP signals. These signals are then led into the TDC for detection. Figure 4.24 shows corresponding TDC output for the detected delay in measurement phase. The measurement results are in accordance with the simulation results.

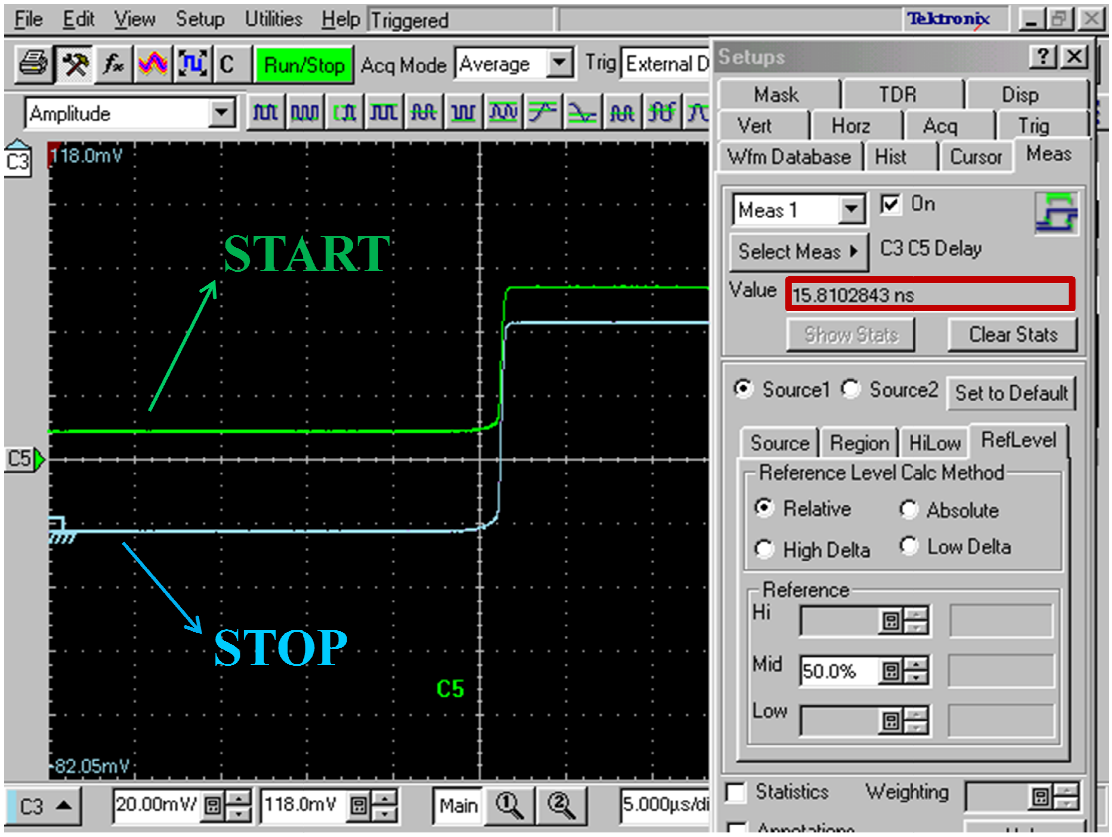


Figure 4.23: The measured relative delay between START and STOP signal, captured using TDS 8000 Digital Sampling Oscilloscope

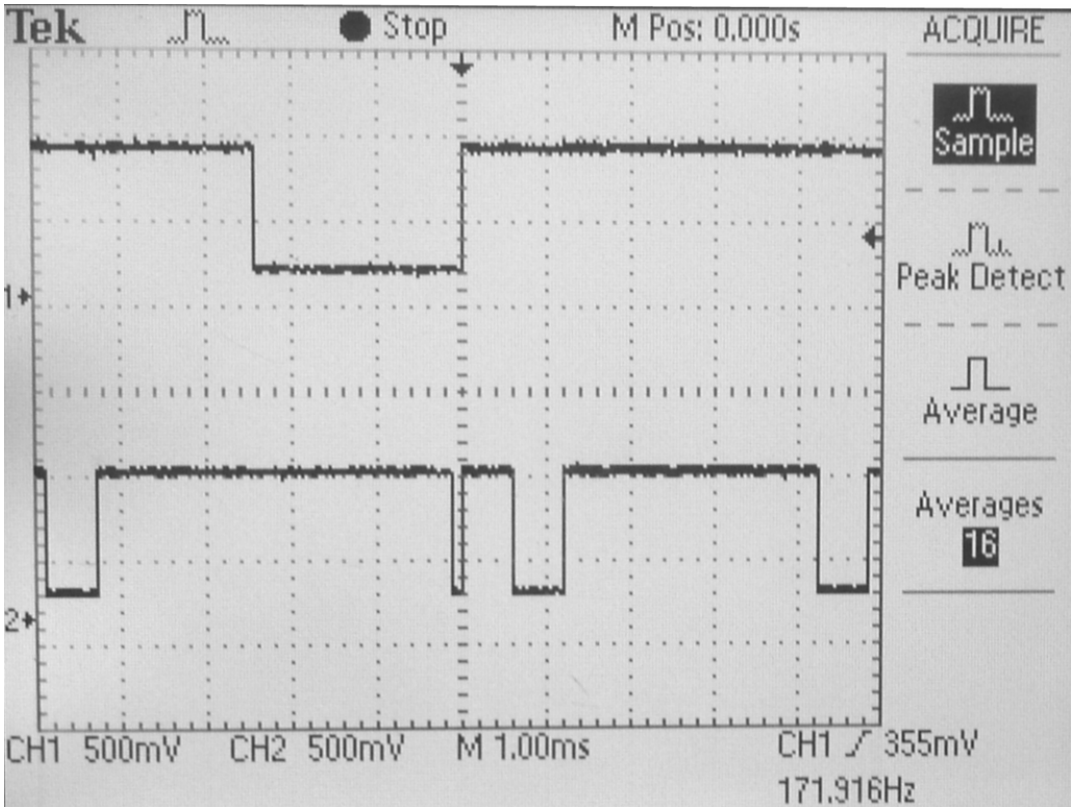


Figure 4.24: Corresponding TDC output for the delay in Fig 4.23

CHAPTER V

CONCLUSION AND FUTURE WORKS

In this work a new readout circuit with integrated BIST scheme for capacitive MEMS devices is proposed. In the proposed scheme instead of commonly used voltage control signals, current controlled stimuli are employed. Using current controlled signals eliminates the risk of MEMS structural collapse in the test phase due to excessive electrostatic force. Thus, hard-to-detect faults can be covered and high fault coverage can be achieved. Variations of MEMS capacitance are first converted to equivalent values of time delay and then converted to digital signal by a time-to-digital converter using a Vernier delay line. The proposed measurement scheme can be self-calibrated to eliminate the need for external calibration equipments. Post layout simulation results indicate that the proposed scheme can successfully be used to detect a wide range of structural defects such as etch variation, broken fingers and stiction. The measurement results using an implemented chip in tsmc65nm technology confirms that.

5.1 Contribution of this work

In this BIST research, a new readout and built-in self-test solution for capacitive MEMS is proposed in which charge controlled stimuli are employed to detect structural defects instead of the voltage sources. Each of the sensitivity and symmetry BIST for voltage control method has been studied. Due to charge control stimuli, proposed BIST scheme covers a larger defect set without risking the structural collapse of the MEMS devices. The control circuit for the readout and BIST implementation consists of some analog MUX and tri-state buffer. Simulations have been performed in Intellisuite CAD

tools on various defects such as missing or broken finger, etch variation and finger height mismatch. The effectiveness of the proposed BIST in detecting these defects based on capacitance variation on fixed capacitance plates is also simulated in CADENCE design tools. Schematic, post layout and measurement results show that the proposed technique is an effective BIST solution for various capacitive MEMS devices. The proposed BIST technique can also be extended to other MEMS devices as well in a similar way.

The proposed BIST method has several advantages over the current voltage-controlled solutions. It has the potential to cover hard-to-detect faults without risking the structural collapse due to excessive electrostatic force; it does not require costly equipments for calibration due to an employed self-calibration technique. The TDC in our BIST solution is self-calibrated through statistical methods reducing the need for costly external instruments in the calibration phase. A reference capacitor was also introduced to reduce the parasitic capacitance effect on the measurement results.

A new technology has been studied and employed for the fabrication of the proposed scheme. TSMC CMOS 65nm technology offers some very new and exciting features which helped a lot in the fabrication phase. The chip is tested for measurement results and they are in accordance with the simulation results. The proposed method has complex circuit design in comparison to the voltage biasing methods and is more sensitive to small variation of input stimulus.

5.2 Future Works

5.2.1 Extension of BIST to other MEMS devices

In this work, MEMS comb accelerometer is used as an example to implement the BIST technique. However, the proposed BIST technique can be extended to other MEMS

devices as well such as Capacitive Micromachined Ultrasonic Transducer. However, due to the complexity of MEMS devices and their working principles, the implementation of BIST remains a very challenging work. This will be left as one of our future research works.

5.2.2 An effective BISR technique

Fault-tolerant or self-repairable MEMS devices are an urgent need of present time. However, MEMS self-repair remains extremely challenging due to its very tiny size. If one segment of the movable part is faulty, it is not feasible to physically remove the faulty part and replace it with a good part. Based on the charge control BIST research, a built-in self-repair (BISR) technique for comb accelerometer devices can be proposed. A control circuit can be integrated inside the modular design of the chip. If any module in the main device is found faulty by the BIST, the control circuit will separate out the faulty module and replace it with a good redundant module. In this way, the device can be self-repaired into good device given the total number of faulty modules is less than the number of redundancy. The developed charge control BIST technique can be used for the testing of each module.

APPENDICES

“Fabrication Steps in tsmc65nm Technology”

The major purpose of this appendix is to introduce the basic usage of a TSMC’s PDK for those users who are completely new to TSMC PDK or never use TSMC’s PDKs before as a reference. To ease the overall introduction, we use a simple TDC design as an example to go through the whole design flow:

- Schematic Capture:

  - Creating library, design, symbol and test fixture.

- Pre-layout Simulation:

  - Using Spectre simulator

  - TDC Performance.

- Layout Creation:

  - Schematic-driven-layout.

  - Component placement.

  - Auto routing.

- Physical Verification:

  - Calibre flow.

- Post-Layout Simulation:

  - Calibre flow.

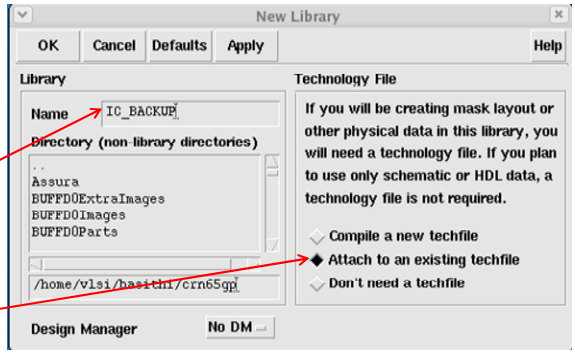
- Schematic Capture:

Creating a Library

- **In the CIW, select *"File->New->Library"***

Enter the new library name into the Name field.

Select *"Attach to an existing techfile"*



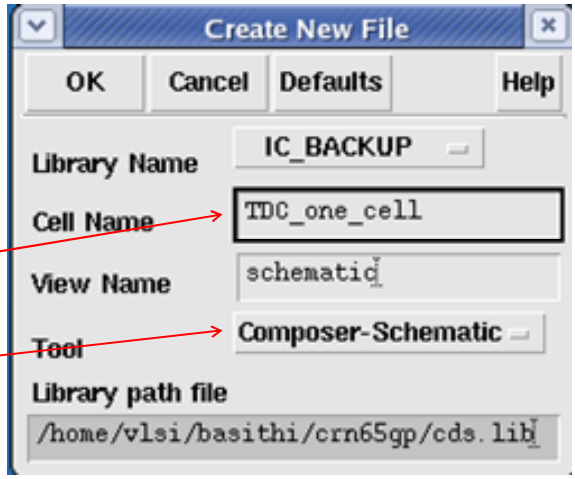
- **In the Attach Design Library to technology file form, select *"tsmcN65"*, and then click OK.**

Creating a Design

- **In the CIW or Library Manager, select "File->New->Cellview"**
- **Setup the Create New File as follows:**

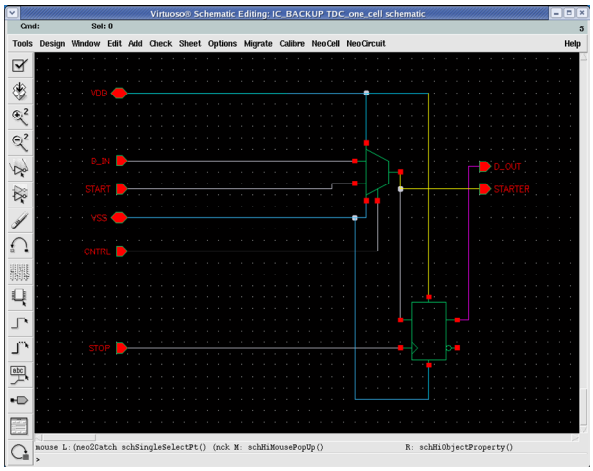
Enter the new cell name into the Name field.
Select "Composer-Schematic"

- **Click OK when done.**



Creating a Design

Build the TDC_1_cell schematic as below:



1.In the TDC_1_cell schematic window, click the *instance* fixed menu icon to display and Add Instance form.

2. Set the *View Name* field in the form to *symbol*.

3.Update the *Library Name*, *Cell Name*, and the property values as in the table on next page as you place each component.

4.After you complete the *Add Instance* form, click *left* on the cursor in schematic window to place that component.

Another way to fill in the *Add Instance* form is to click on the *Browse* button. This button opens up a *Library Browser* from which you can select the components to place your left mouse button.

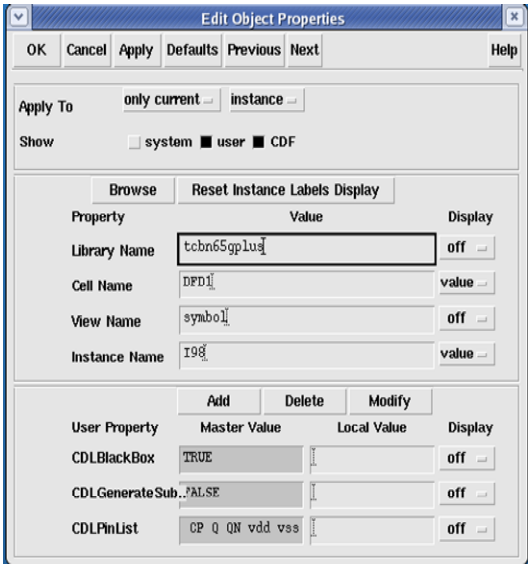
Creating a Design

Component	Library Name	Cell Name
MUX	tcbn65gplus	MUX2D0
D-Filp-Flop	tcbn65gplus	DFD1

If you place a component with wrong parameter values, you can use the,

Edit->Properties->Objects

command to change the properties.

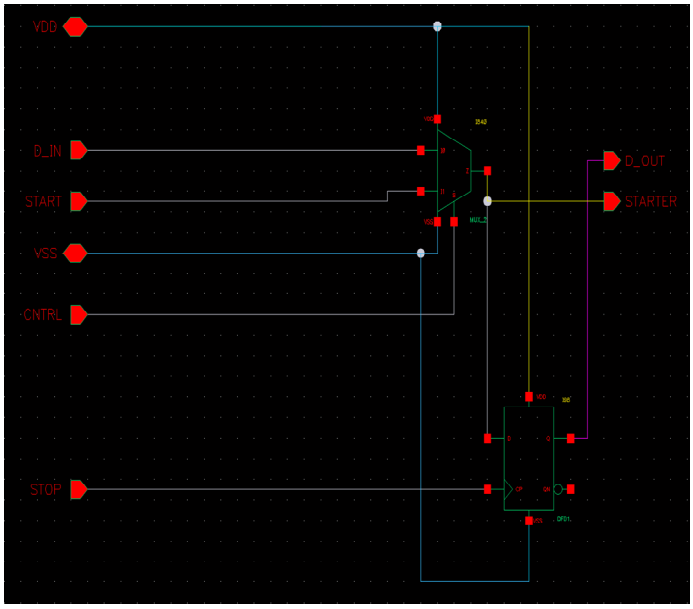


Creating a Design

1. After entering components, add following Pins from the schematic window:

VDD, VSS, D_IN, START, STOP, CNTRL, D_OUT, STARTER

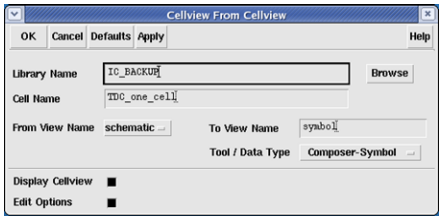
2. The final schematic should look as shown in the side.



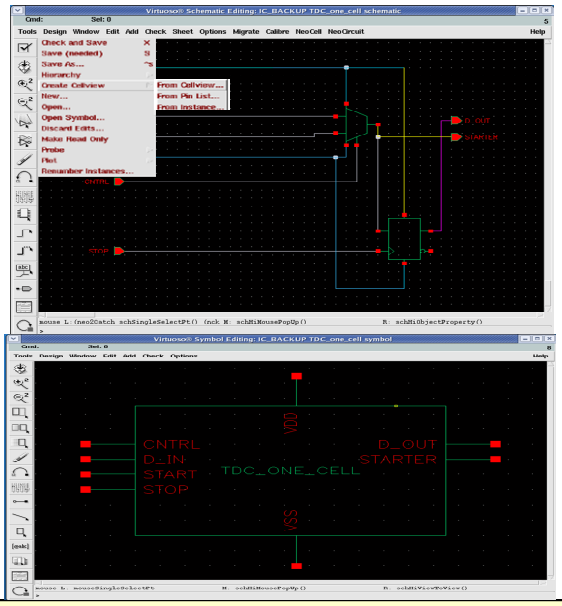
Creating a Symbol

After schematic capture, we need to create corresponding symbol for it.

1. In the TDC_1_cell schematic window, select *"Design->Create Cellview>From Cellview"*
2. Setup the *Cellview From Cellview* window as below:



3. Click *OK* then the symbol view is created: →

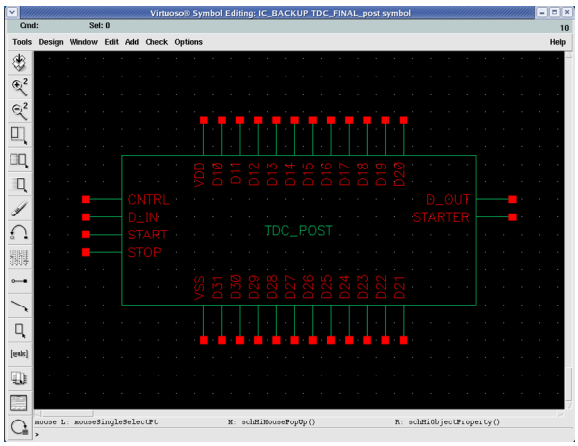


Creating a Test Fixture

The final step before we start the simulation is to create a test fixture. Generally the test fixture will consist of the following components: a core design (the TDC_1_cell in our case), voltage source, ground and other input values as in table.

- **For our test purpose we have added 32 of the TDC_1_cell symbols to create a full TDC.**

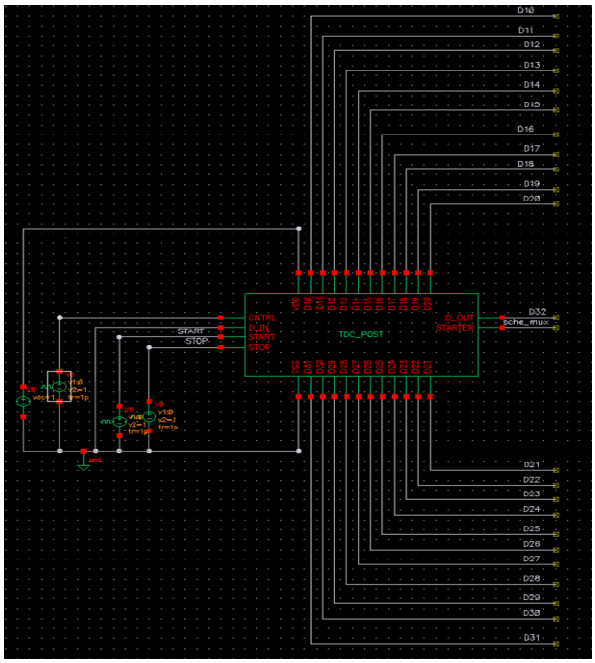
Library	Cell	Properties
analogLib	vdc	For VDD=1V
analogLib	gnd	For VSS=0V
analogLib	vpulse	For CNTRL
analogLib	vpulse	For START
analogLib	vpulse	For STOP
analogLib	vpulse	For D_IN



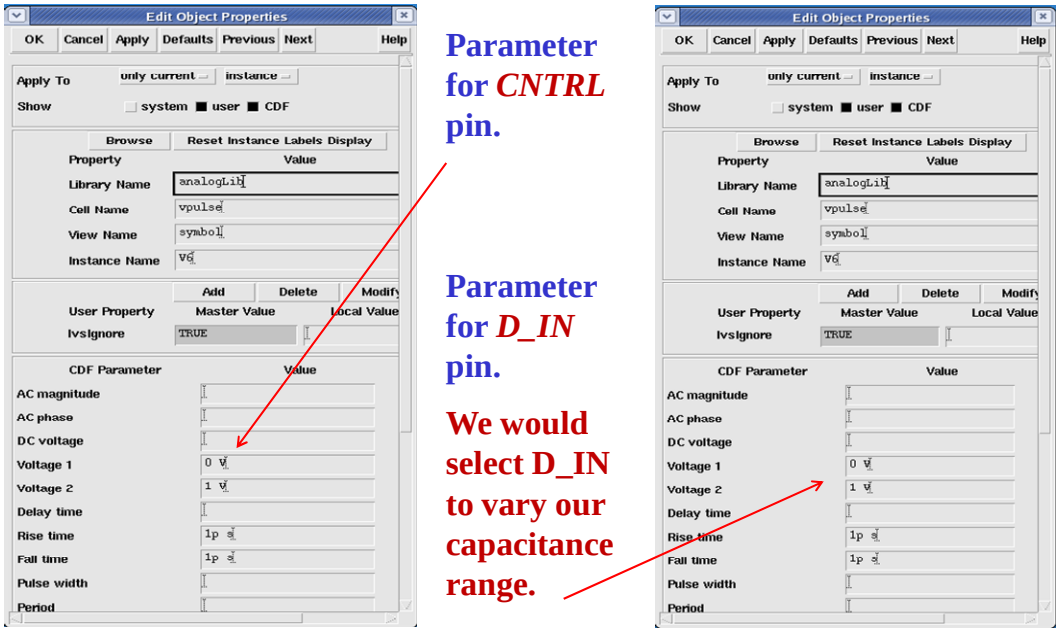
Symbol of a full-TDC

RESEARCH CENTRE FOR INTEGRATED MICROSYSTEMS - UNIVERSITY OF WINDSOR

Creating a Test Fixture

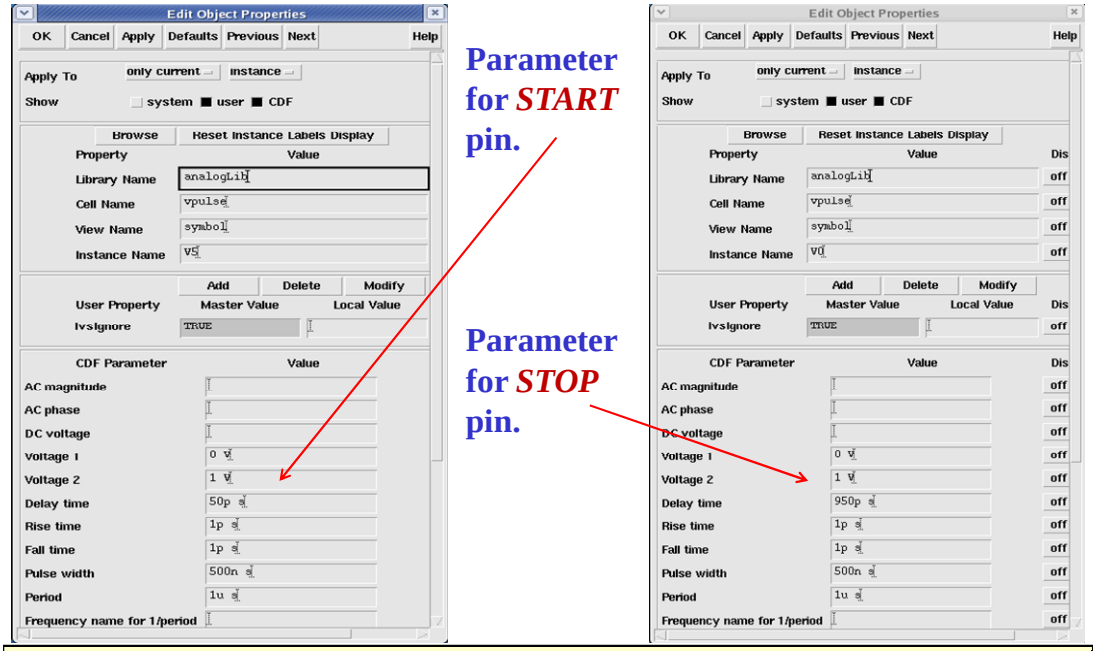


Creating a Test Fixture



RESEARCH CENTRE FOR INTEGRATED MICROSYSTEMS - UNIVERSITY OF WINDSOR

Creating a Test Fixture



- Pre-layout Simulation:

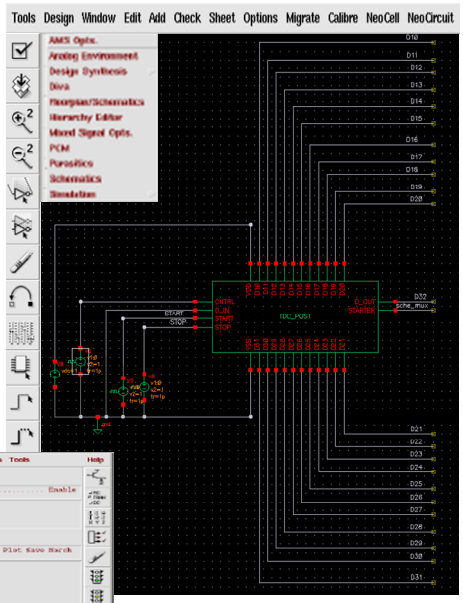
Pre-layout Simulation

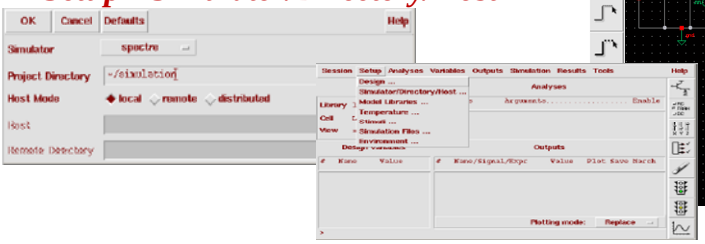
1. We will simulate our design with *spectre simulator* using *Analog Artist* environment. In the menu banner of *"TDC_final"* schematic view:

"Tools->Analog environment"

2. Set *Simulator* to *spectre* and specify *"Project Directory"*. In the *Analog Artist* window:

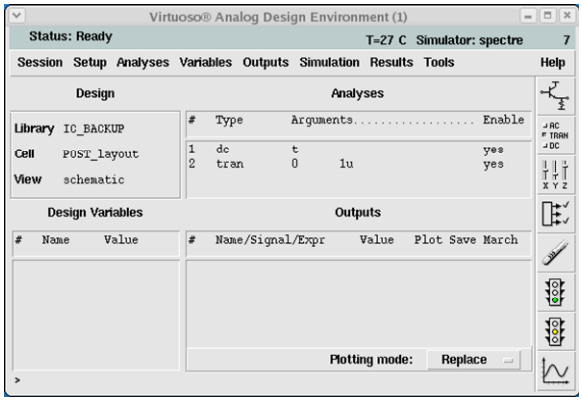
"Setup->Simulator/Directory/Host"

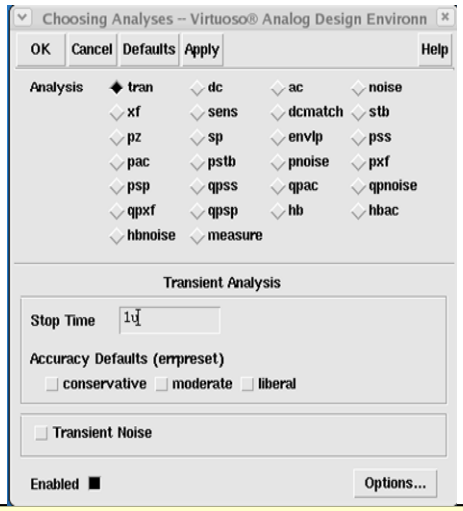




Using Spectre simulator

1. Select analysis type and fill in parameters for simulation.

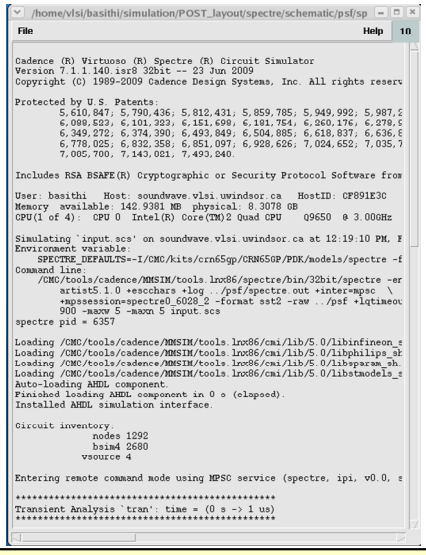


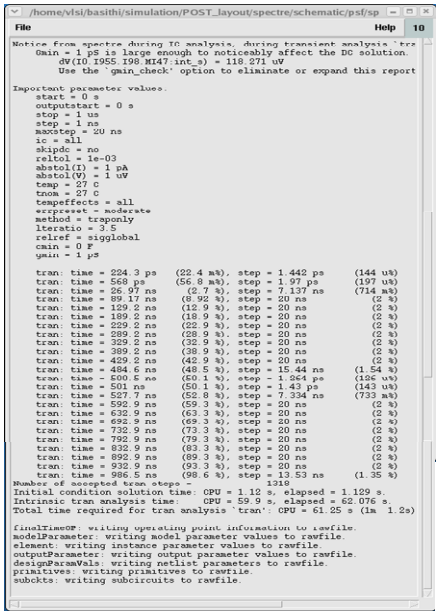


2. Setup of *tran* analysis.

Using Spectre simulator

Run simulation, click *"simulation->netlist and run"*

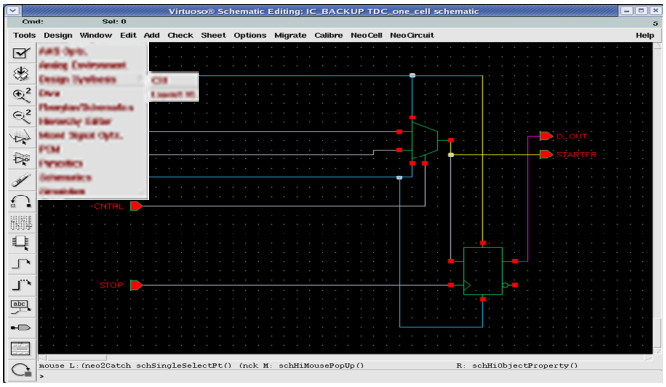


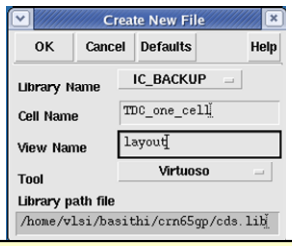


- Layout creation:

Layout Creation

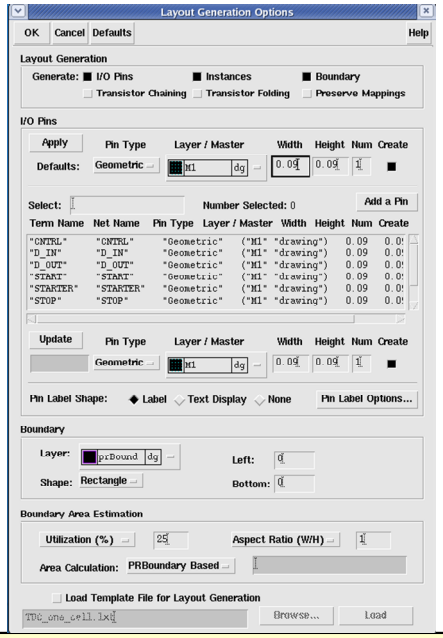
1. **From schematic menu select *"Tools->Design Synthesis->Layout XL".***
2. **In the dialog box input the cell name and view name for the layout, a new Virtuoso XL layout window should pop out.**
3. **From Virtuoso XL layout menu select *"Design->Gen from source".***



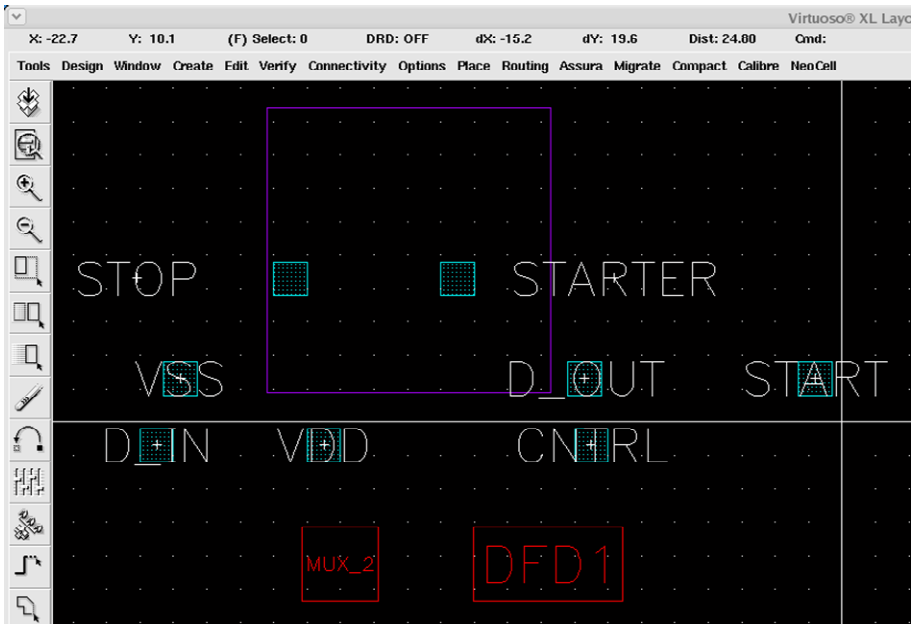


Schematic-Driven-Layout

4. A layout generation options window appears and prompts users to setup the ***pin layers, pin width, pin height, boundary layer***....and so on for required layout generation.
5. Please refer to the figure beside for required input for basic layout generation. →
6. When clicked OK, you should see some rectangle representing the components.

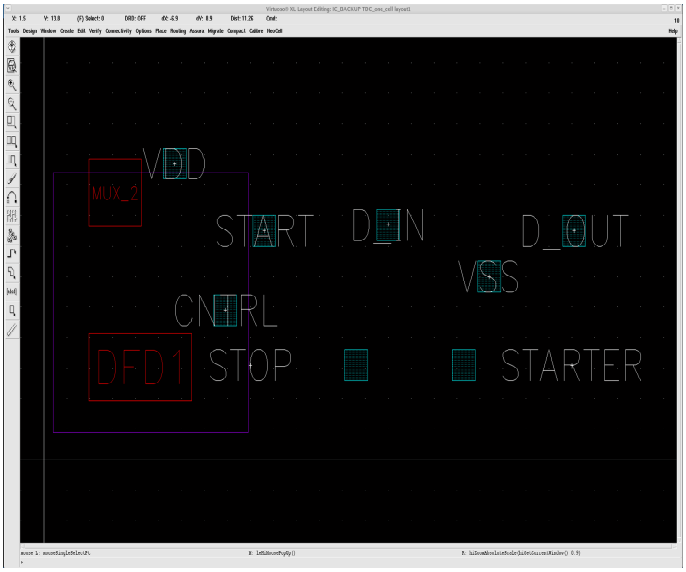


Initial Layout View



Component Placement

1. The components now have to be placed inside the cell boundary, click *"Edit->Place As In Schematic"* in the layout window.
2. Select and drag the devices/IO pins to proper location. Look for the lines representing the *connections* of selected object to other objects.



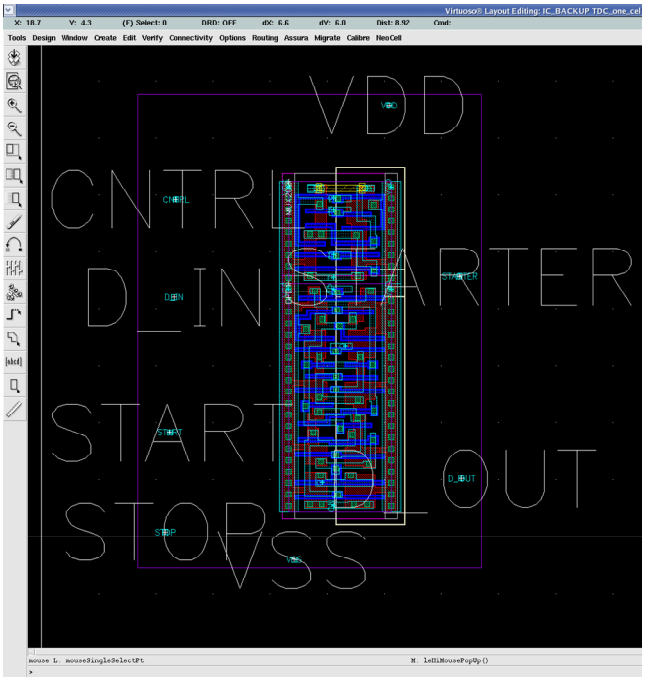
Configuring I/O Pins

1. In LSW window select layer to *M1-pin*. ←

2. In the Virtuoso Layout window click *"create->label"* and input the same name as the I/O pins. →

Final Layout (Before Routing)

Please check, the pins (colored white and blue)have to be inside the layout boundary (in violet). The pin names (in white) are zoomed big just for easy pickings.

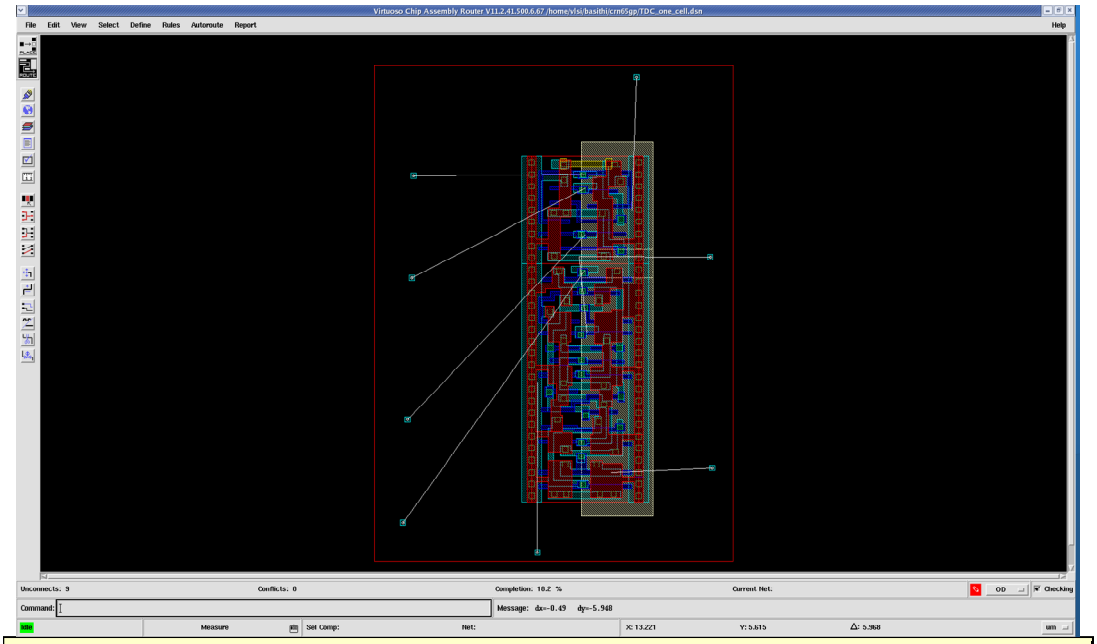


Auto Routing

Once the setup is complete, we send the design for auto routing.

1. In the Virtuoso Layout window click *"router->export to router"*.
2. Fill up the required value as shown beside and click *OK*.
3. A new window will pop up as shown in the next slide.

Auto Routing Continued..

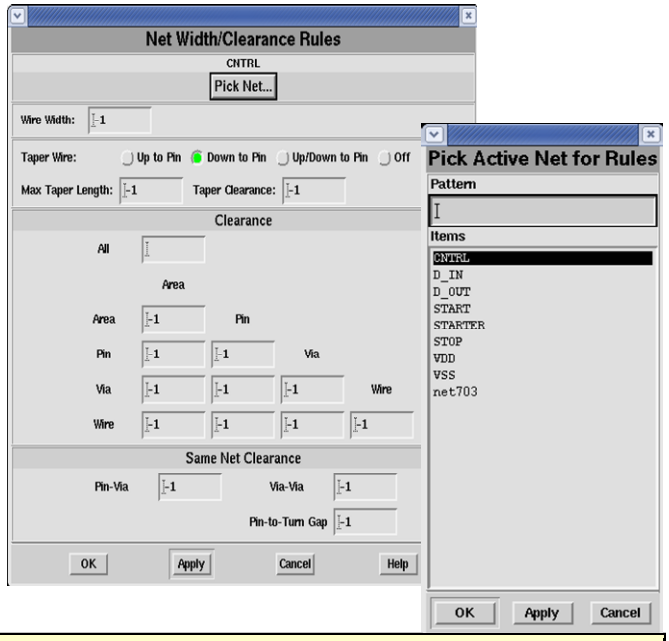


RESEARCH CENTRE FOR INTEGRATED MICROSYSTEMS - UNIVERSITY OF WINDSOR

Auto Routing Options

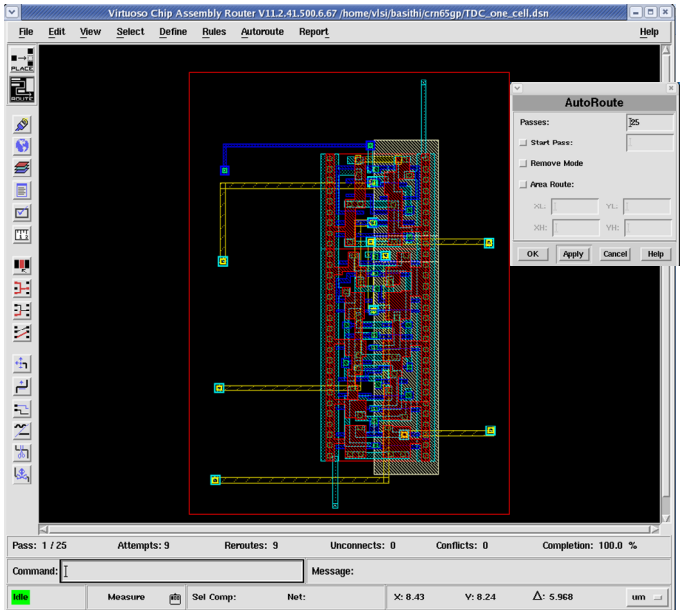
There are several Options that we can play with before sending the design for final routing.

1. Click *"Rules->Net->Width/Clearance"*.
2. We can change the path width and spacing between them as required.
3. We can play with other parameters of interest like Noise, Crosstalk, Shielding etc.

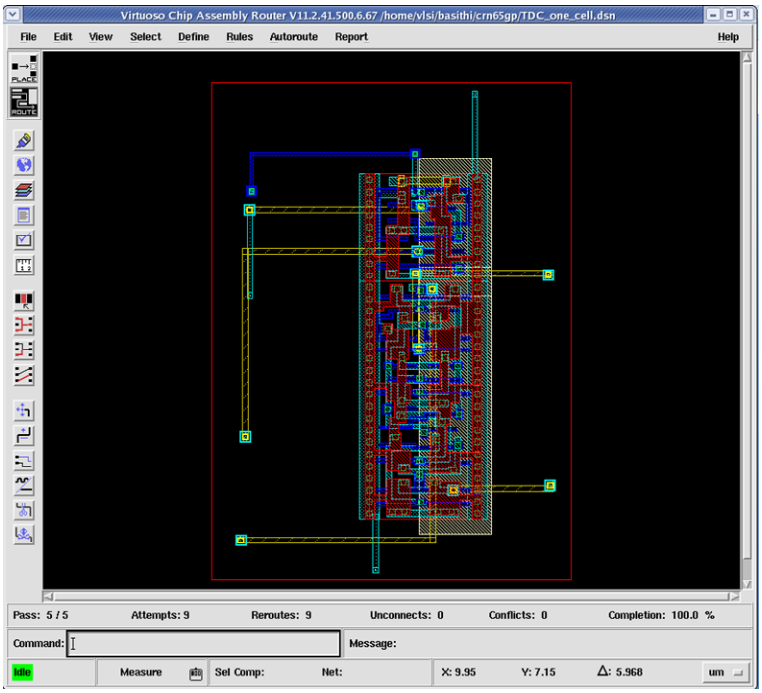


Auto Routing

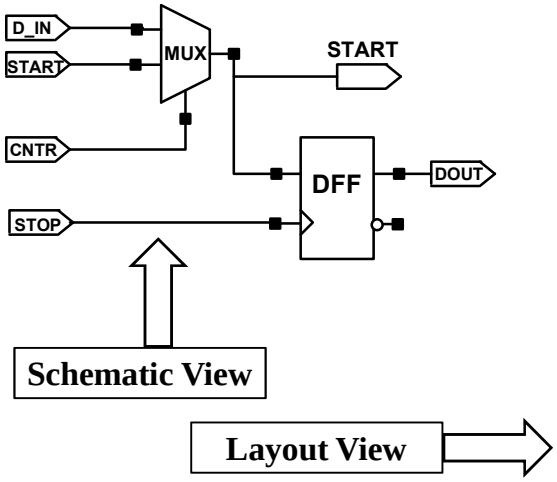
1. Click *"Autoroute->Detail Route->Detail Router"*.
2. Define the number of passes and click OK.
3. The auto-routed design will appear.
4. You may click *"Autoroute->Clean"* and this will fine tune the routing.
5. Click *"Quit and Save"* and the routed design will appear on top of the un-routed layout window.

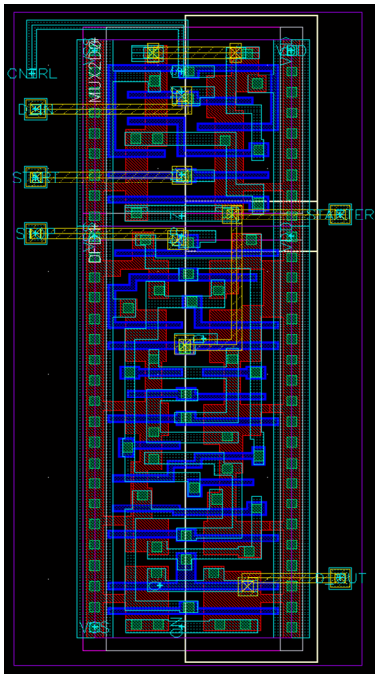


Auto Routing

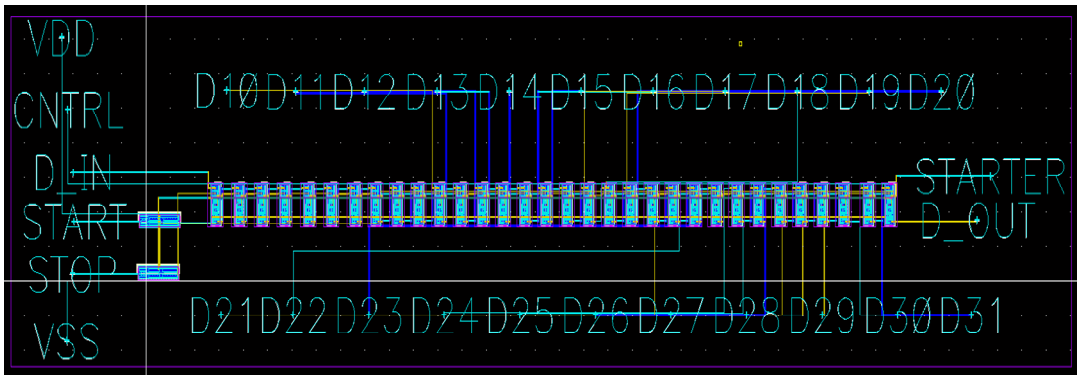


TDC – Single Cell Layout view, after routing





Full TDC – Layout View After auto routing



- Physical Verification:

Physical Verification

After layout creation and routing is completed we have to perform following physical verifications

1. DRC (Design Rule Check): **Make sure the design is error free and eligible to be fabricated through manufacturers.**

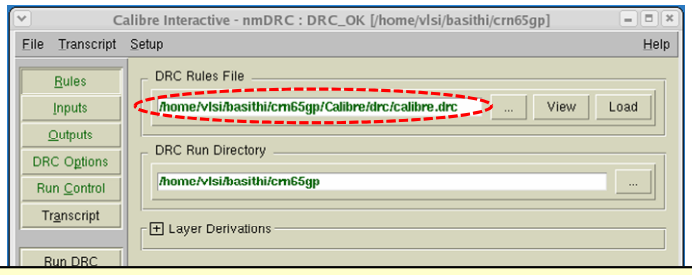
2. LVS (Layout Versus Schematic): **To ensure each device in the layout is in complete match to its corresponding schematic.**

3. PEX/RCX (Parasitic Extraction): **To perform post layout simulation and make sure the design work well after taking the parasitic R & C effects into account.**

Calibre DRC Flow

Calibre DRC mode flow works under Cadence Virtuoso environment.

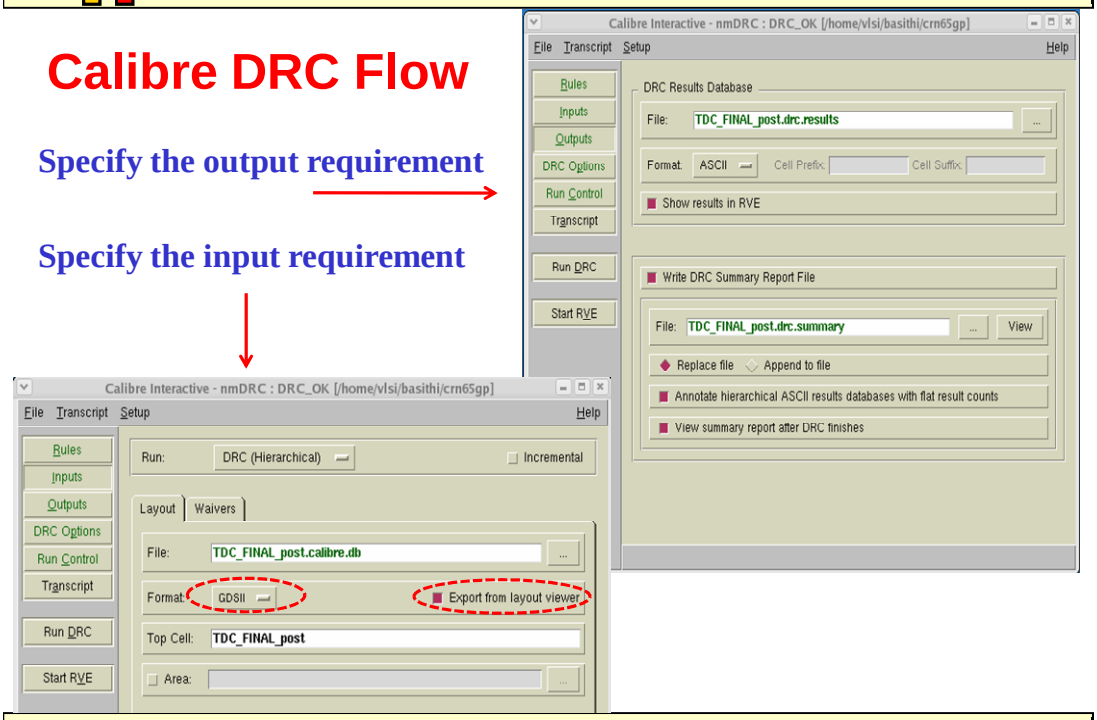
1. **Click *"Calibre->Run DRC"***
2. **Specify the rules file.**
3. **Check the input and output tabs for your requirement.**
4. **Click *"Run DRC"* and check the result in RVE.**
5. **If the layout is not DRC free, re-edit the layout and re-run the DRC.**



Calibre DRC Flow

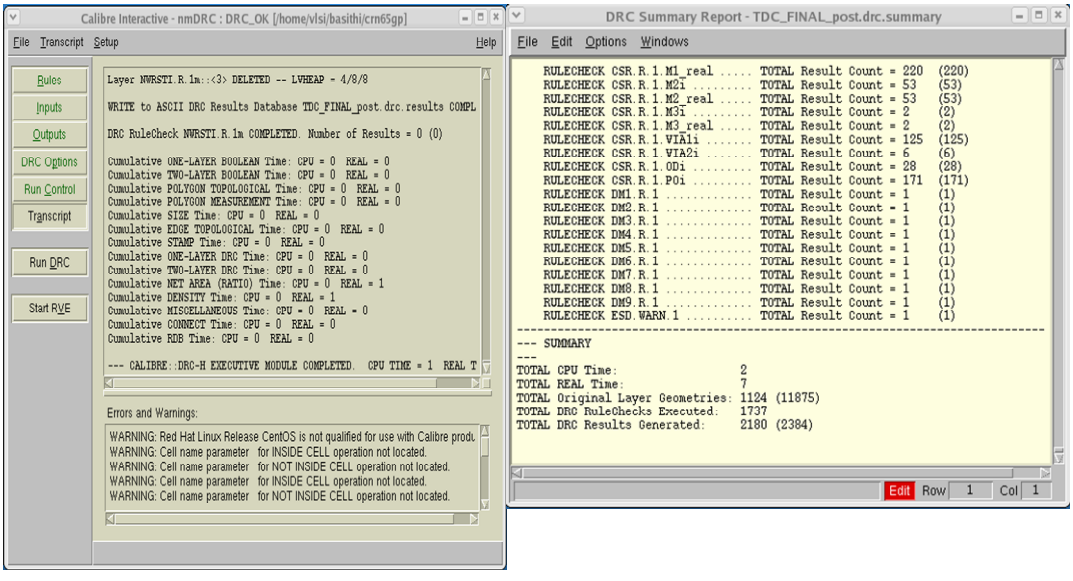
Specify the output requirement →

Specify the input requirement ↓

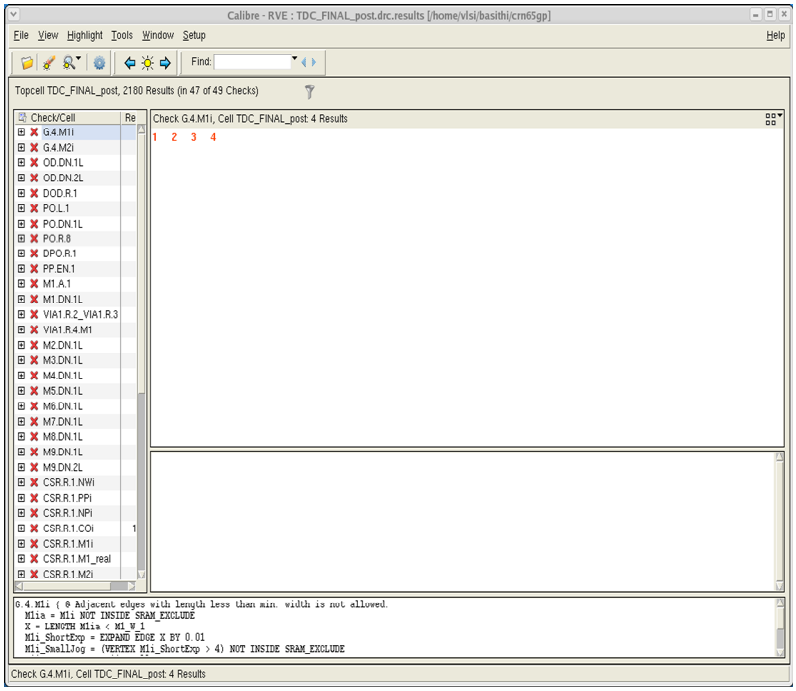


RESEARCH CENTRE FOR INTEGRATED MICROSYSTEMS - UNIVERSITY OF WINDSOR

Calibre DRC Flow



Calibre DRC Warnings



DRC shows the layout almost pass the DRC except for some density and reliability rule.

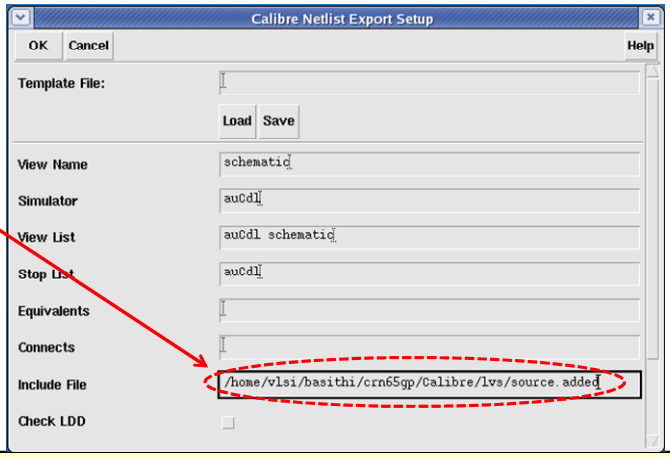
RESEARCH CENTRE FOR INTEGRATED MICROSYSTEMS - UNIVERSITY OF WINDSOR

Calibre LVS Flow

After no DRC violation, LVS check make sure the layout is a complete match to the schematic.

1. **First you have to specify the empty sub-circuit file "source. added" file provided along with the LVS deck.**

2. **Click *"Calibre->Setup->Netlist Export"*.**

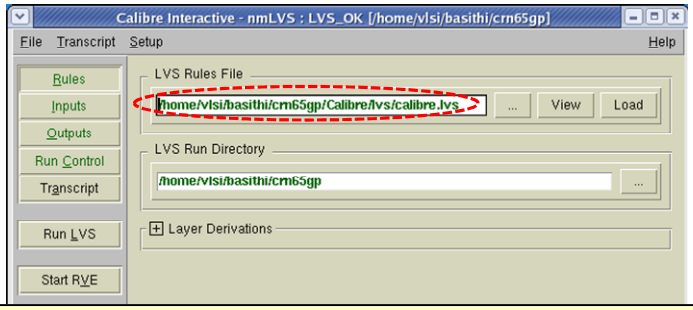


3. **Click *"Calibre->Run LVS"* to invoke the new user interface.**

Calibre LVS Flow

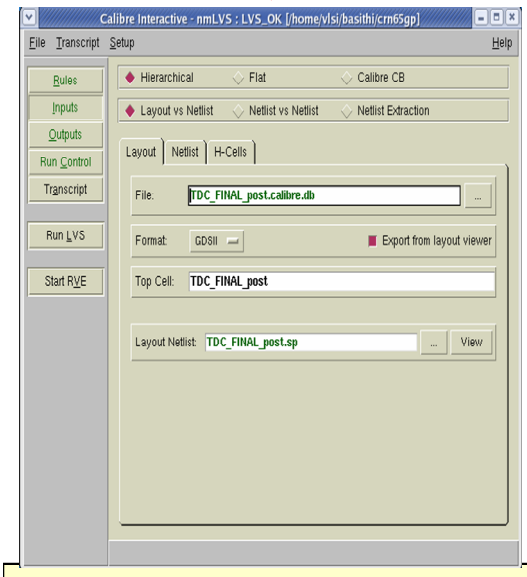
Calibre DRC mode flow works under Cadence Virtuoso environment.

1. **Specify the LVS rules file.**
2. **Check the input and output tabs for your requirement.**
3. **Click *"Run LVS"* and check the result.**
4. **If the layout is not matched to schematic, re-edit the layout and re-run the LVS check.**

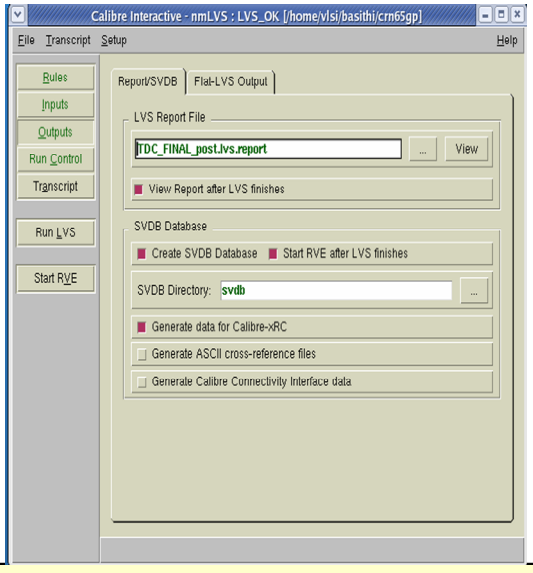


Calibre LVS Flow

Specify the input requirement ↓

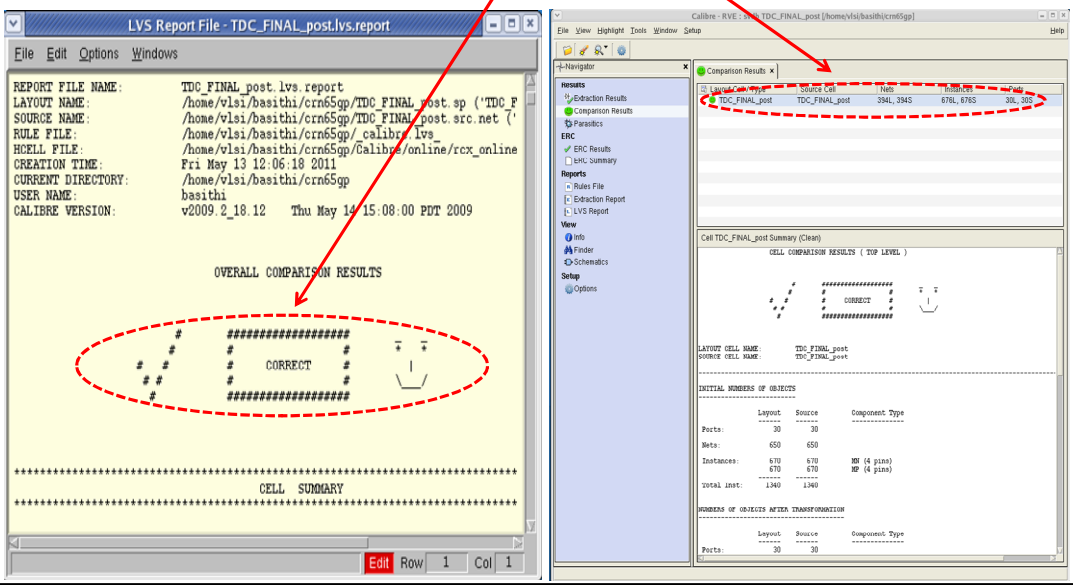


Specify the output requirement ↓



Calibre LVS Flow

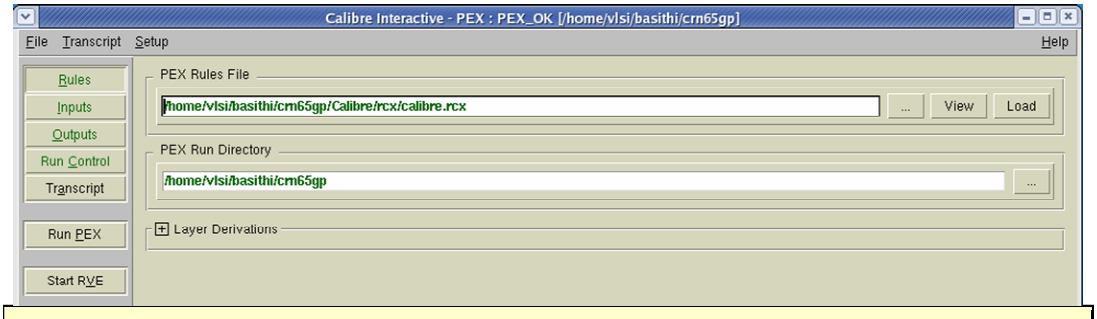
Below is the good result showing LVS match.



Calibre PEX Flow

When the layout is verified to be DRC free and LVS clean, we need to perform the parasitic RC extraction.

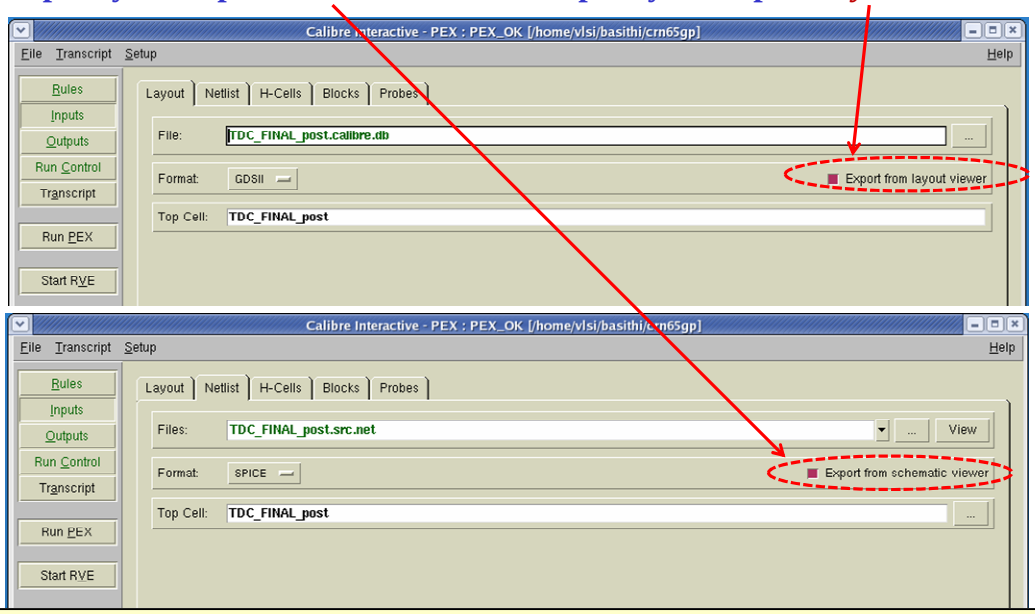
1. **Click *"Calibre->Run PEX"*.**
2. **Specify the PEX rules file.**
3. **Check the input and output tabs for your requirement.**
4. **Click *"Run PEX"*.**



Calibre PEX Flow Input

Specify the input *"Netlist"* tab

Specify the input *"layout"* tab

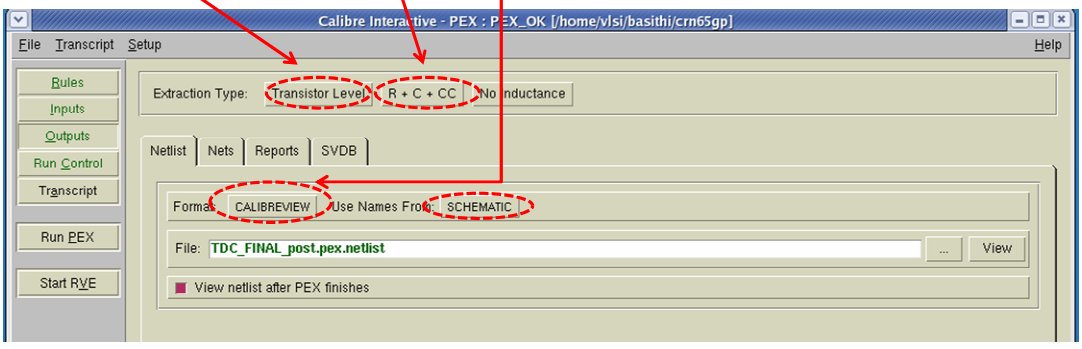


Calibre PEX Flow Output

Select which extraction you want

Select the output format

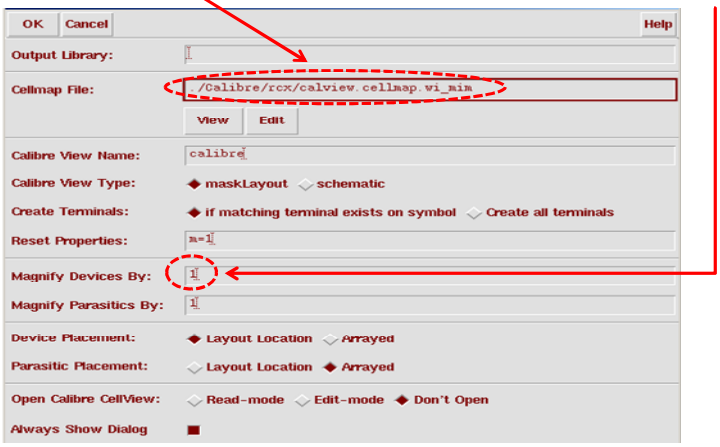
Set the extraction type



Calibre PEX Flow

When the extraction run is completed, a calibre view setup window pops up.

1. **Specify the *"Cellmap File"* and *"Magnify Devices By"*.**



2. **Click OK to create the Calibre view.**

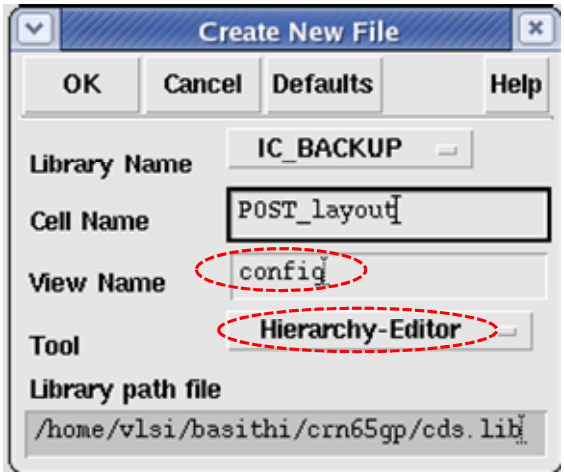
- Post Layout Simulation:

Post Layout Simulation

When the physical verification is OK, and layout was extracted, we need to perform the post layout simulation. This time, not only the original components but also the parasitic R & C of the interconnections are taken into consideration. Hence, this result is much closer to the real silicon measurement data. So it is obvious the pre-layout and post-layout simulation results will not be the same. As a matter of fact, post layout simulation would add some delay, and START and STOP signals would show up with a bit of delay in comparison with the schematic simulation.

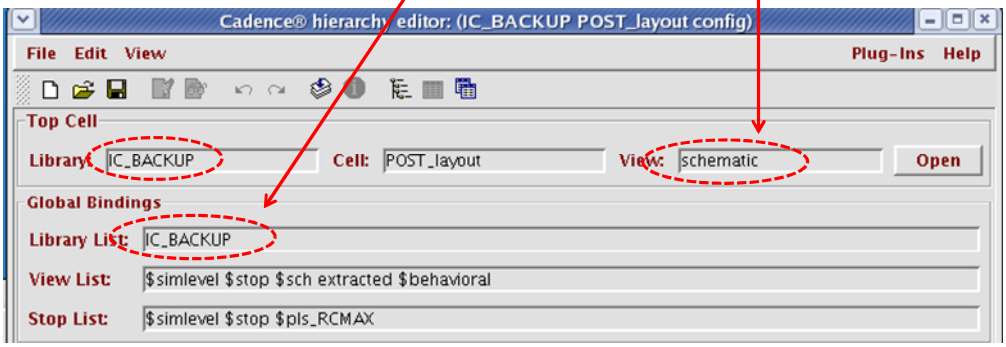
Post Layout Simulation

1. In the library manager, select *"File->New->Cellview"*.
2. Setup the *Create New File* form as follows:



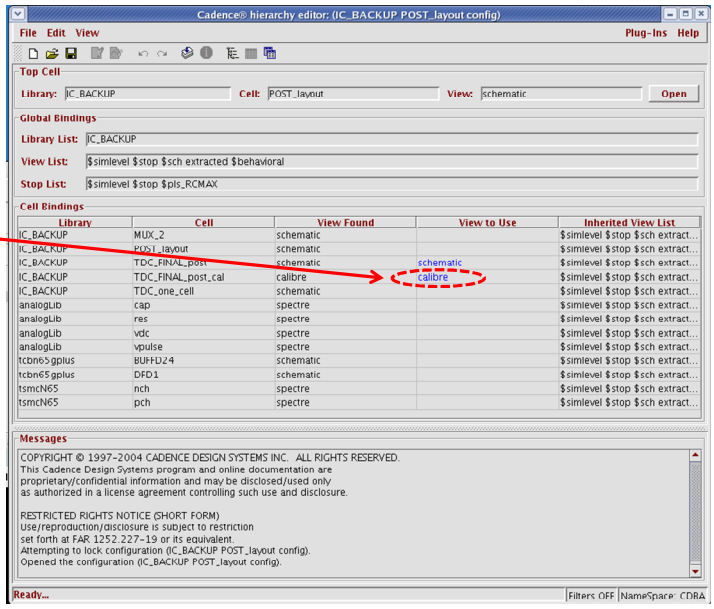
Post Layout Simulation

3. At the top of the form select view to *"schematic"* and at the bottom click on the *"Use Template"*.
4. In the Use Template form, select the name to *"Spectre"*.
5. Change the default library name to your library.



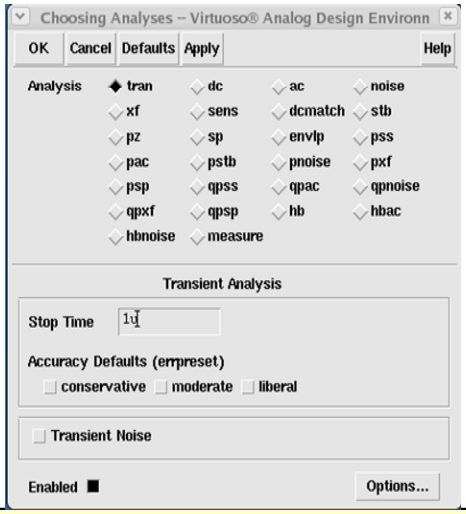
Post Layout Simulation

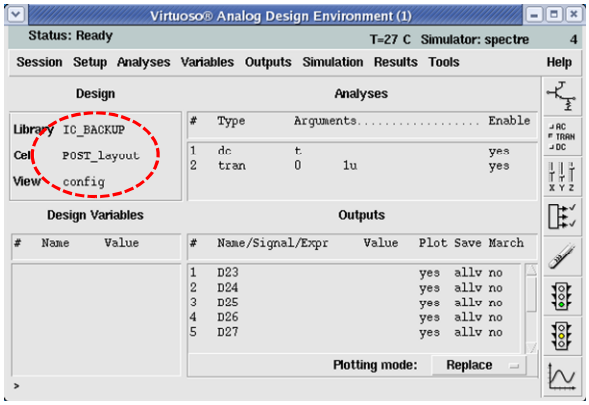
6. Edit the hierarchy for the design by changing the *"View to Use"* To Calibre.



Post Layout Simulation

1. Select analysis type and fill in parameters for simulation. View name should be *config*.





2. Setup of *tran* analysis.

REFERENCES

[1] L. S. Fan, Y. C. Tai and R. S. Muller, “IC-processed electrostatic micro-motors”, *IEEE International Electron Devices Meeting. Technical Digest*, pp. 666-669, 11-14 Dec. 1988.

[2] Baltes, O. Brand, G. K. Fedder, C. Hierold, J. Korvink and O.Tabata, “CMOS-MEMS: Advanced Micro and Nanosystems”, Wiley-VCH, 2005.

[3] W. Kuehnel and S. Sherman, “Modeling of the Mechanical Behavior of a Differential Capacitor Acceleration Sensor,” *Sensors Actuator A: Physics*, vol. 48, no. 2, pp. 101-108, May 1995.

[4] Nilmoni Deb, and R.D. Blanton, “Built-In Self-Test for CMOS-MEMS Accelerometers,” in Proc. *International Test Conference*, pp. 1075-1084, October 2002.

[5] B. Charlot, S. Mir, F. Parrain, and B. Courtois, “Electrically induced stimuli for MEMS self-test,” in Proc. *19th IEEE VLSI Test Symp.*, May 2001, pp. 210–215.

[6] M. Aikele, K. Bauer,W. Ficker, F. Neubauer, U. Prechtel, J. Schalk, and H. Seidel, “Resonant accelerometer with self-test,” Sensors Actuators,A: Physical, vol. 92, pp. 1–3, 2001.

[7] Xingguo Xiong, Yu-Liang Wu, and Wen-Ben Jone. “A Dual-Mode Built-In Self-Test Technique for Capacitive MEMS Devices” in *IEEE Transactions on Instrumentation and Measurement*, vol-54, No. 5, pp. 1739-1750, Oct 2005.

[8] International technology roadmap for semiconductors, Technical report, Semiconductor industry association, 2010.

[9] B. V. Amini and F. Ayazi, “A 2.5 V 14-bit Sigma-Delta CMOS SOI Capacitive Accelerometer,” *IEEE J. Solid-State Circuits*, vol-39, No. 12, pp. 2467-2476, Dec. 2004.

[10] B. V. Amini, S. Porkamali, and F. Ayazi, “A high resolution, Stictionless, CMOS Compatible SOI Accelerometer with a Low Noise, Low Power, 0.25-μm CMOS interface,” in *Proce. IEEE International Conference on MEMS*, 2004, pp. 572-575.

[11] B. V. Amini and F. Ayazi, “Micro-gravity Capacitive Silicon-on-Insulator Accelerometers,” *J. Micromech. Microeng.*, 2005, vol. 15, pp. 2113-2120.

[12] Navid Yazdi, Haluk Kulah, and Khalil Najafi, “Precision Readout Circuits for Capacitive Microaccelerometers,” in *Proceedings of IEEE conference on Sensor,* pp. 28-31, Oct 2004.

[13] S.J. Sherman, et.al., “Low cost monolithic accelerometer”, *Dig. VLSI Circuits Symp.,* June 1992, pp. 34-35.

[14] K. Chau, S.R. Lewis, Y, Zhao, R. T. Howe, S.F. Bart, and R.G. Marcheselli, ”An integrated force-balanced capacitive accelerometer for low-g applications,” 1995 *IEEE Conf. on Solid-State Sensors & Actuators,* June 1995, pp. 593-596.

[15] J. Wu, G.K. Fedder, L.R. Carley, “A low-noise low-offset capacitive sensing amplifier for a 50-μg/√Hz monolithic CMOS MEMS accelerometer”, *IEEE J. of Solid-State Circuits*, vol. 39, May 2004, pp. 722-730.

[16] W. Yun, R.T. Howe, and P.R. Gray, ”Surface micromachined digitally force-balanced accelerometer with integrated CMOS detection circuitry,” *Solid-State Sensor and Actuator Workshop,* Hilton-Head Island, SC, USA, June 1992, pp. 126-131.

[17] J. A. Geen, S. J. Sherman, J. F. Chang, S. R. Lewis, “Singlechip surface micromachined integrated gyroscope with 50°/h Allan deviation,“ *IEEE J. of Solid-State Circuits*, vol. 37, Dec. 2002, pp.1860-1866.

[18] N. Yazdi, A. Mason, K. Najafi, K.D. Wise," A generic interface chip for capacitive sensors in low-power multiparameter microsystems," *Sensors & Actuators Part A,* vol. 84, Sep. 2000, pp. 351-361.

[19] N. Yazdi, K. Najafi, "An interface IC for a capacitive silicon μg accelerometer," *1999 IEEE Int. Solid-State Circuits Conf.,* Feb. 1999, pp. 132-133.

[20] N. Wongkomet, B. E. Boser, "Correlated double sampling in capacitive position sensing circuits for micromachined applications," *1998 IEEE Asia-Pacific Conf. on Circuits and Systems,* Nov. 1998, pp.723-726.

[21] M. Lemkin, B. Boser, "A three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *IEEE J. of Solid-State Circuit,* vol. 34, April 1999, pp. 456-468.

[22] H. Kulah, J. Chae, N. Yazdi, K. Najafi, "A multi-step electromechanical sigma-delta converter for micro-g capacitive accelerometers," *2003 IEEE Int. Solid-State Circuits Conference,* Feb. 2003, pp. 202-203.

[23] R. Rashidzadeh, M. Ahmadi and W. C. Miller, "An All-Digital Self-Calibration Method for a Vernier-Based Time-to-Digital Converter," in *IEEE Transactions on Instrumentation and Measurement,* vol-59, issue-2, pp. 463-469, Feb 2010.

[24] Henry V. Allen, Stephen C. Terry, and Diederik W. De Bruin, "Self-Testable Accelerometer Systems," in *IEEE Proceedings of Micro Electro Mechanical Systems,* pp. 113-115, Feb 1989.

[25] Nilmoni Deb, and R.D. Blanton, "Multi-Modal Built-In Self-Test for Symmetric Microsystems," in *IEEE Proceedings of VLSI Test Symposium,* pp. 139-147, Apr 2004.

[26] A. Chatterjee and R. Voorakaranam, "Test Generation for Accurate Prediction of Analog Specifications," Proc. 18th IEEE VLSI Test Symp. (VTS 00), IEEE CS Press, 2000, pp. 137–142.

[27] W. Kuehnel and S. Sherman, “A surface micromachined silicon accelerometer with on-chip detection circuitry,” *Sensors Actuator A: Physics*, vol. 45, no. 1, pp. 7-16, Oct. 1994.

VITA AUCTORIS

Objectives: To obtain a research and development position in electrical engineering/computer science/information technology department in an institution where my teaching, research and leadership skills would be effectively utilized with an opportunity for advancement.

Citizenship: Canadian Permanent Resident.

Professional Profile:

- Three years of university teaching and research and one year of industry research experience.
- Excellent research and communication skills within university, and industry through conducting research on developing BIST (Built-In Self-Test) solution for MEMS devices funded by NSERC and CMC.
- Three accepted conference papers in the area of BIST for MEMS devices, and DIB (Device Interface Board), one submitted paper in NEMS and one submitted IEEE transaction which demonstrates my commanding written skills.
- Attended many conferences, and presented my work overseas which proves my strong verbal skills.
- Possess excellent interpersonal, communication and leadership skills and collaborative team spirits that helped perform duties successfully as VP – Finance (2011-2012) and as ECE departmental representative (2009-2010) in Graduate Student Society at University of Windsor.

Education:

1. University of Windsor, Windsor, ON, Canada

Master of Applied Science (M.A.Sc.) Sep 2009- Aug 2011

- Major: Electrical and Computer Engineering
- GPA: 12.25/ 13.00 (Letter Grade: A)
- Supervisor: Dr. Majid Ahmadi and Dr. Rashid Rashidzadeh
- Thesis: 'A new BIST solution for MEMS devices based on charge control technique'
- Work: I have proposed and implemented a novel BIST solution for capacitive MEMS sensors based on charge controlled technique. The IC is fabricated by CMC (Canadian Microelectronics Corporation) using tsmc65nm technology.

2. Shahjalal University of Science and Technology (SUST), Sylhet, Bangladesh

B.Sc. Engineering Dec 1997- Dec 2001

- Major: Computer Science and Engineering
- Result: First Class First with ***honors*** in a class of 62.
- CGPA: 3.85/ 4.00 (Letter Grade: A)
- Exam held and Degree awarded: Dec 2004

Research Interests:

- Analog, Mixed-signal, and RF devices, MEMS devices and testing.
- Signal and Image Processing, Image Segmentation, VLSI circuit design.
- Database, and Web applications, multimedia.

Professional Membership:

2010- Present, Student Member, Institute of Electrical and Electronics Engineers (IEEE)

Professional Experiences:

1. Graduate Assistant, Research Assistant

M.A.Sc. in Electrical and Computer Engineering, Univ. of Windsor

Sep 2009- Aug 2011

Responsibilities include:

- Conducting tutorial classes and laboratory experiments, grading quizzes, assisting instructors in the administration of examinations.
- Assisting project coordinator as well as the supervisor with the development and implementation of project work plans; assisted in the clarification of objectives and operational needs to facilitate project implementation.
- Conducting literature reviews (searching and locating appropriate prior research related to project content and methodology; abstracting articles for literature review, writing drafts of project report sections related to prior research).
- Assisting with data collection activities (survey development, collecting, organizing, and analyzing project data, research information related to project or proposal content and methodology; presenting information in appropriate format to support project/research objectives; writing section of proposals and reports; preparing and distributing special reports requested by funding agencies).
- Developing new methods based on literature review, performing laboratory experiments and simulations, compiling the experimental observations.

- Assisting professors in the analysis of results and preparation of articles for international conferences and journals.
- Attending research group seminars and make a presentation on the research progress.

2. Shahjalal University of Science and Technology (SUST), Sylhet, Bangladesh

Jan 2006- May 2007

Project Lead, Open Source Migration for Ministry of Cultural Affairs (MoCA) of Bangladesh, Funded by government of Peoples Republic of Bangladesh

- I lead a dynamic team that worked to upgrade the whole IT section of MoCA to Open Source.

3. Shahjalal University of Science and Technology (SUST), Sylhet, Bangladesh

Jan 2006- May 2007

Project Lead, Full Bengali Database of Freedom Fighters of 1971 of Bangladesh, Funded by government of Peoples Republic of Bangladesh

- Worked with a group of students and analyzed, processed and prepared a complete database in Unicode for the Ministry of Liberation War Affairs where all freedom fighter's records (around 144500 entries) are taken from the official gazette of Bangladesh.

4. Shahjalal University of Science and Technology (SUST), Sylhet, Bangladesh

Jan 2006- May 2007

Project Manager, Codewitz Asia link Project (Ref. BD Asia-Link/10/095-229), Funded by European Union, Co-coordinating Partner- Computer Science and Engineering Department.

Codewitz Asia-Link Project-for better programming skills- A project funded by the European Union where the main project coordinating partner was the Tampere Polytechnic, Tampere, Finland and other partners were the University of Applied Sciences Berlin, Germany and Bangladesh University of Engineering and Technology, Dhaka, Bangladesh.

- Conducted research for developing programming skills both for undergrad students and teachers.
- Prepared budget, equipment purchase, and setup research lab, developing plans, designing and implementing learning objects.
- Prepared progress reports to the main coordinating partner as well as the European Union.

5. Shahjalal University of Science and Technology (SUST), Sylhet, Bangladesh

Jan 2006- Apr 2007

Instructor, Postgraduate Diploma in Information Technology, Funded by Ministry of Science and Information & Communication Technology, Government of People's Republic of Bangladesh, Co-coordinating Partner- Computer Science and Engineering Department.

Postgraduate Diploma in Information Technology (PGD-IT) - A program financed by the Ministry of Science and Information & Communication Technology, Government of the

People's Republic of Bangladesh and conducted by the Computer Science and Engineering Department, Shahjalal University of Science and Technology, Sylhet, Bangladesh.

- Monitor performance against project baseline and maintain project documentation
- Guide and assist the project team in the development of the project plan.
- Mentor others who wish to develop competence in project planning and control.
- Obtain and process status data and maintain an updated plan.
- Evaluate project status and performance. Recommend appropriate corrective actions.
- Develop and maintain standards for planning and control

6. Shahjalal University of Science and Technology (SUST), Sylhet, Bangladesh

Nov 2005- June 2007

Lecturer, Computer Science and Engineering Department

Main responsibilities included teaching, research, administration and management.

- Taught Operating System, Data Communication, Computer Networking, Digital Signal Processing and Lab using Matlab, System Analysis and Software Engineering, Analog Communications, Digital Electronics, Numerical Analysis using Matlab, Data Structure and Algorithm, Discrete Mathematics, Introduction to Computer Application, Fundamentals of Electrical Engineering, Electric Circuits I and II, Introduction to Programming in C/C++.
- Supervised 3rd year and 4th year student's projects. Followed up the student's progress on bi-weekly basis and gave direction to solve the engineering problem

by applying the engineering theory. Attended student's seminar as a committee member and a supervisor.

- Proctoring exams, examination committee member, and result processing, grading scripts and worked as an advisor for undergrad students, course and program assessment committee
- Executive Member of the departmental procurement committee and Laboratory Setup Committee, Curriculum review committee, University Website Development Committee and University Computer Center.

7. Leading University, Sylhet, Bangladesh

Jan 2005- Nov 2005

Lecturer, Computer Science and Engineering Department

Main responsibilities included teaching, research, administration and management.

- Taught Software Engineering, Data Structure and Algorithm, Introduction to Computer Application, Introduction to Programming in C/C++.
- Supervised 4th year student's projects. Followed up the student's progress on bi-weekly basis and gave direction to solve the engineering problem by applying the engineering theory.
- Proctoring exams, examination committee member, and result processing, grading scripts and worked as an advisor for undergrad students, course and program assessment committee.

8. Shahjalal University of Science and Technology (SUST), Sylhet, Bangladesh

June 2006- June 2007

CCNA Instructor (On Leave), SUST Regional Academy

Responsibilities include:

- Taught students how to configure routers and gateways, TCP/IP configuration settings, higher level protocol design etc.

Publications:

1. Built-In Self-Test for Capacitive MEMS Using a Charge-Controlled Technique, Iftekhar Ibne Basith, Nabeeh Kandalaft, and Rashid Rashidzadeh, published in IEEE 19th Asian Test Symposium, Shanghai University of Science and Technology, Shanghai, China, December 1-4, 2010.
2. A New BIST Architecture for MEMS Fault Detection, Iftekhar I. Basith, N. Kandalaft, R. Rashidzadeh and M. Ahmadi, presented in the 2010 CMC TEXPO Research Competition in Ottawa, Ontario, Canada, October 4-6, 2010.
3. A MEMS Based Device Interface Board, N. Kandalaft, I. Basith, and R. Rashidzadeh, published in the 2010 International Test Conference in Austin, Texas, October 31 - November 5, 2010.
4. High Speed Test Interface Module using MEMS Technology, N. Kandalaft, I. Basith, R. Rashidzadeh, and M. Ahmadi, accepted in the IEEE International Symposium on Circuits and Systems in Rio de Janeiro, Brazil,

May 15 - 18, 2011. (withdrawn)

5. A New Integrated Readout and BIST Solution for MEMS Sensors, Iftekhar I. Basith, N. Kandalaft, R. Rashidzadeh and M. Ahmadi, accepted in the CMC TEXPO research competition 2011, October 19-20, 2011, Gatineau, QC, Canada.
6. A New Integrated Readout and Built-in Self-Test Method for Capacitive MEMS using a Charge Control Technique, Iftekhar Ibne Basith, Nabeeh Kandalaft, Rashid Rashidzadeh and Majid Ahmadi, submitted in the *Transaction of Computer Aided Design (TCAD)*, September 10, 2011.
7. Performance Enhancement of Single Electron Junction 1-bit Full Adder, Iftekhar Ibne Basith, Tareq Muhammad Supon, Ajit Muhury, Rashid Rashidzadeh, Majid Ahmadi, submitted in the IEEE ICECS 2011 in Beirut, Lebanon, December 11-14, 2011.

Scholarships/ Awards:

- Winner of **Ontario Graduate Scholarship (OGS)** for Ph.D study in Electrical Engineering from Fall 2011.
- Winner of **Dr. Ross Paul Scholarship** for academic achievement in post graduate level.
- Coach of SUST's ACM ICPC programming team (Ranked 11th among about 70 teams in 2006 Regional Programming Contest in Coimbatore, Chennai, India).
- Winner of Prime-Minister Gold Medal award, Chancellor’s gold medal and Vice-chancellor’s silver medal for extra-ordinary academic career in SUST.

- Awarded the best foreign speaker and emerging youth leader in International Youth Jam, 2006 in Karachi, Pakistan for a speech on distance learning and digital divide.

Academic Projects:

- **CPPLL**: Charge Pump Phase Locked Loop was designed and performance was verified. (2010)
- **CMUT**: Design and implementation of hexagonal CMUT (capacitive micromachined ultrasonic transducer) as part of advanced MEMS project which earned me A+ and huge appraisal. (2010)
- **OpAmp**: Design and performance analysis of an Operational Amplifier (OpAmp). (2009)
- **Full Adder**: Design and implementation of full adder using SET (single electron) devices as part of nanoelectronics project work. (2009)
- **Designing WAP site for e-governance**: My supervised group developed a WAP site which allows the citizens of Sylhet City Corporation to pay governmental bills (Electricity, phone, gas, tax) by pre-paid card using HTML, WML, PHP, JavaScript, MySql. (2006)
- **Face Tracking Software:** Designed and implemented using matlab with a group of students. Earned 2nd prize in software fair in Dhaka, Bangladesh. (2006)
- **Diskless Cluster Computing:** As part of the final year project, using LINUX OS, and net booting concept implemented a diskless cluster of 16 PC's which was highly appreciated. (2004)

- **Designing the Fiber-Optic backbone for SUST:** Me and my course teacher laid out the network design for our university and also a portion of small village back in Bangladesh. (2003)
- **Design and Implementation of Admission System in SUST:** One of my supervised groups did this job, which was also highly appreciated. (2006)
- **AIRP: AN IP Anycast Protocol Approach:** One of my supervised group worked on the inter-domain IP anycast routing for IPv6 network and proposed a modification of existing interior routing protocol. (2007)
- **Banking Database Management System in Java:** Designed and developed a complete database driven system for a bank as a course project. (2002)

Academic Research Experience/ Skills:

- Highly efficient knowledge of C/C++, Java, relational databases, matlab, Oracle, PL/SQL and Linux.
- Extensive knowledge of industrial design CAD tools like Intellisuite, Cadence, SIMON and HFSS.
- Very Good experiences in solving algorithmic and mathematical problems using various data structures and algorithms.
- CCNA instructor training in Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh.
- Presented research outcome to the weekly seminar at Research Center for Integrated Microelectronics (RCIM), University of Windsor since September 2009. Results are discussed with other students and professors.

- Teaching undergraduate courses as part of my GA duties since September 2009 for average class size around 40/50 students.
- Attended Ontario Skills Symposium organized by the Canadian Federation of Students as part of GSS.

Extra-curricular Activities:

- **Elected Positions:**
    1. **Vice President - Finance** in Graduate Student Society in 2011-2012, University of Windsor, Windsor, ON, Canada.
    2. **Graduate Student Representative** in Graduate Student Society in 2009-2010, Electrical and Computer Engineering Department, University of Windsor, Windsor, ON, Canada.
    3. **Student Affairs Secretary** in Bangladesh Canada Association of Windsor-Essex for 2009-2010.
    4. **General Secretary** of Computer Science and Engineering (CSE) Society, SUST, Bangladesh in 2002-2003, elected by huge margin by e-voting.
- **Chairing Committees:** I have chaired numerous technical meetings related to course design, examination committee, and project planning during my endeavors with university.
- **Project Management:** During my university teaching tenure at Shahjalal University of Science and Technology I was team lead for four top priority projects. Three of them were financed by different Ministries in Government of People's Republic of Bangladesh and the other was financed by European Union. I was involved from

early stage of procurement of these projects. My responsibility included liaison with management, and different teams within the project, and optimizing man, material, machine, and money involved in the project, cash flow management and risk management.

- Won a US State Department scholarship to study as a short-term scholar at Washington College in Maryland for a short summer term (summer 2004)
- Taught and trained numerous student groups for programming contests focusing on data structures and algorithms design and implementation.
- Led departmental football and basket ball team to championship once, and runner-up thrice in SUST, Bangladesh.
- Was involved in fund-raising and relief distribution activities during floods in 1998 and 2004 in Bangladesh along with local government.